Compact Frontend–Electronics and Bidirectional 3.3 Gbps Optical Datalink for the H1–Experiment

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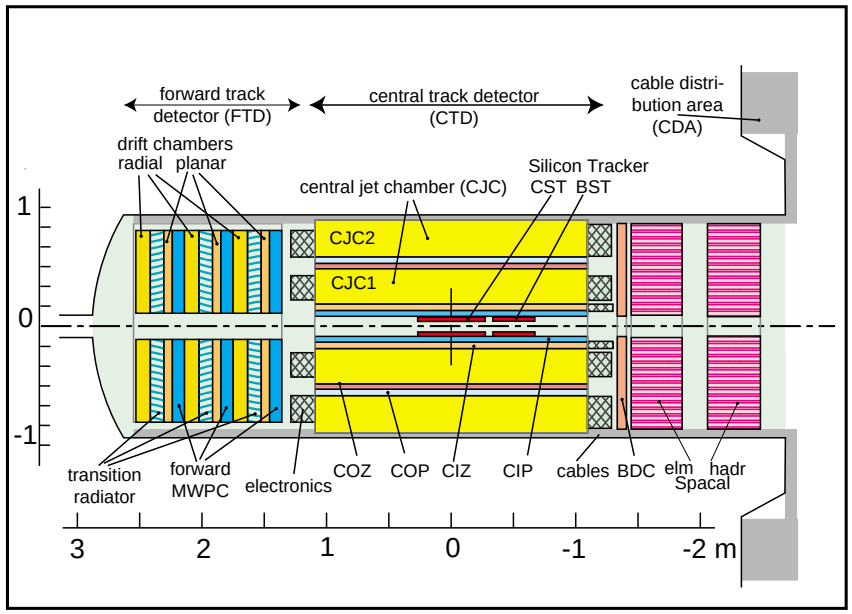
- Motivation
- The Design
- Performance
- Optical Links for LHC Experiments
- Conclusions and Outlook

Motivation : Y2k H1 Upgrade



- Increase in luminosity by factor 5 anticipated
- L1–Eventrate (now): 1 kHz,
  Backgroundrate (now): 50 to 500 kHz
- Even higher p–wall / –gas reactions

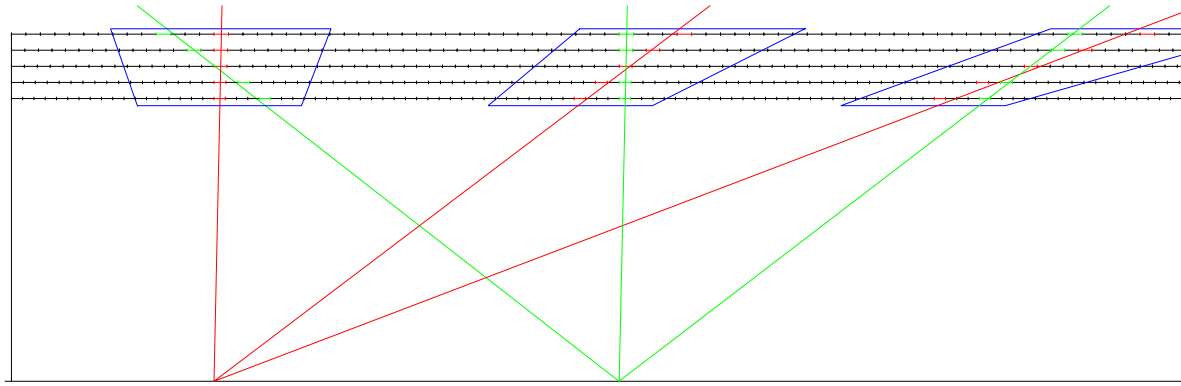
  ⇒ Improve z–vertex trigger

  ⇒ Rebuild Central Inner MWPC (CIP)

New CIP :

5 layers from $r = 152...198$ mm
with 16 segments in azimuth
max. 119 pads per segment along z–axis

⇒ ∼9600 channels



Motivation : Constraints

Read out of 9600 pads :

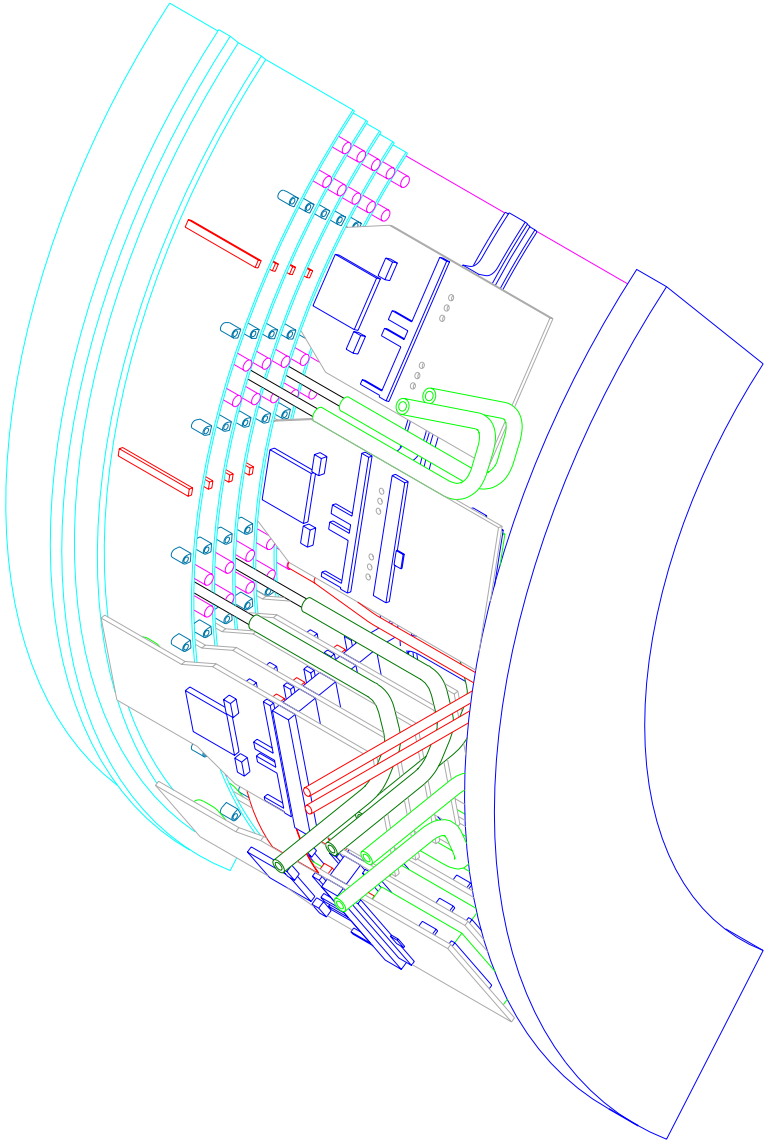
- p and e meet every 96 ns
- 100 Gbps information to be transmitted to trigger electronics 40 m away
- Low contribution to dead material budget

$\Rightarrow$ Optical transmission data link

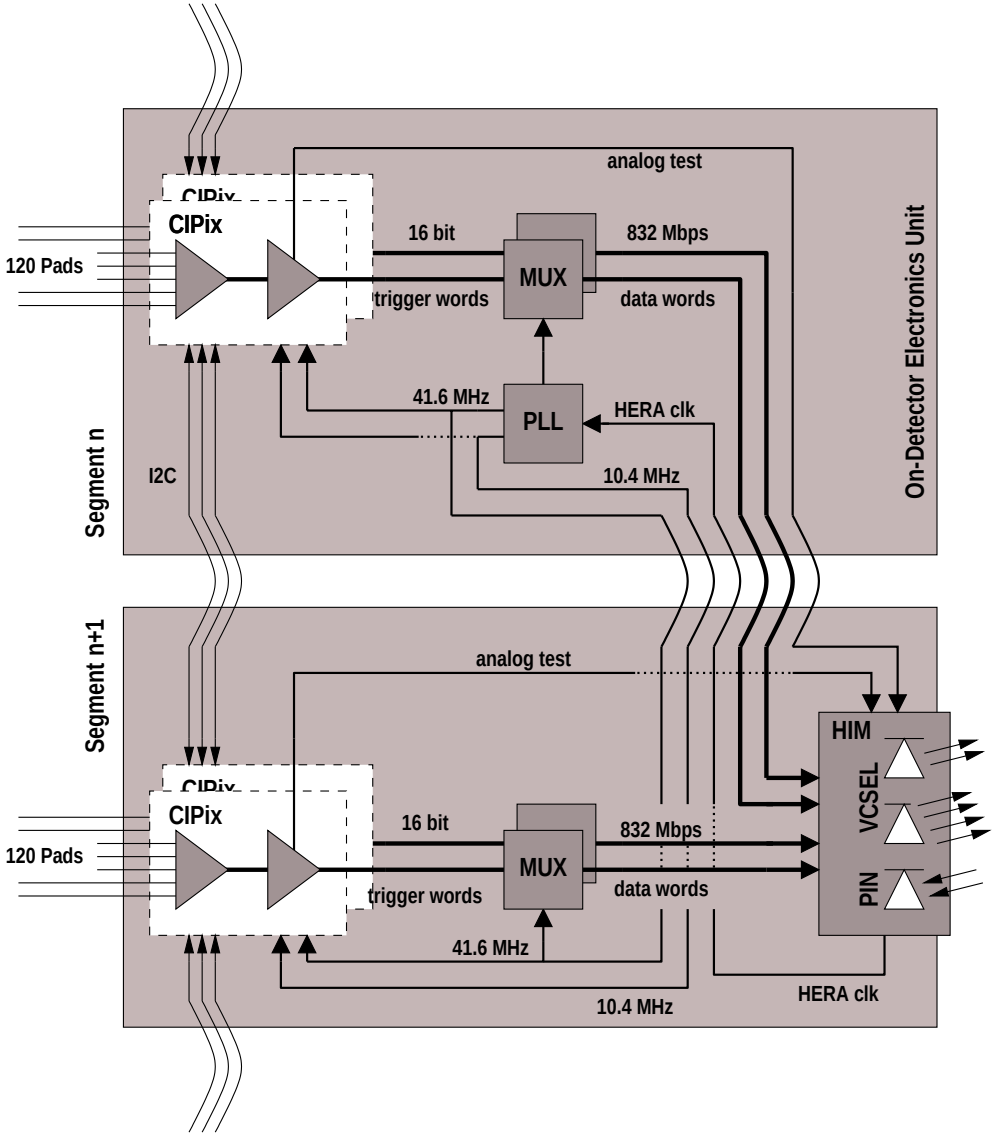
Very tight spatial constraints :

- Must fit into existing environment (together with LV & HV cables, cooling & gas lines, support structures)
- Heat dissipation has to be minimized

$\Rightarrow$Compact frontend electronics



Design : Frontend–Electronics



For each 60 pads :

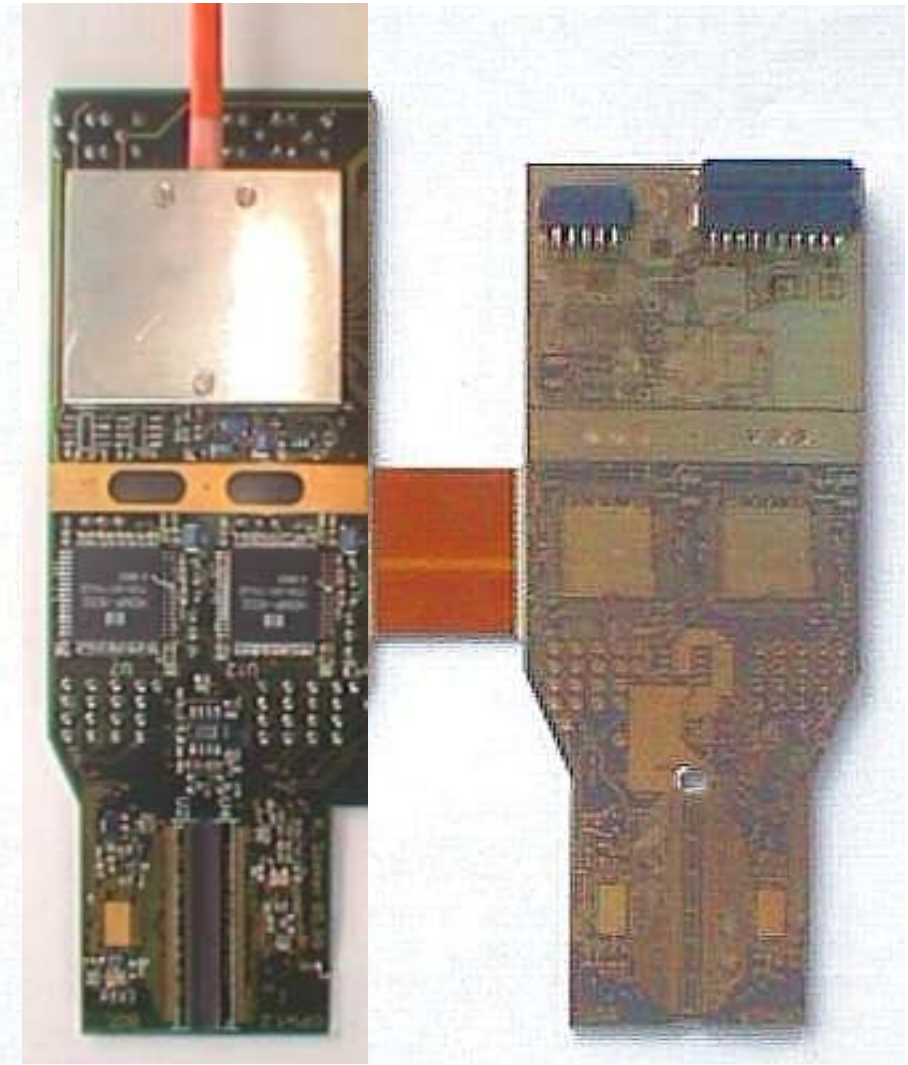
- CIPix amplifies, shapes, discriminates and 4–fold multiplexes
  → 4×15 bit *trigger word*
- 1 bit *first word tag*
- HP 16–fold multiplexer HDMP–1032 addes 4 bit *encoding word* and serializes
  → 832 Mbps (4×20 bit *data word*)
- Analog pad information can be selected via I^2C bus and exported

⇒ To be transmitted :
4×832 Mbps digital & 2× analog signals

- Global HERA clock for synchronisation

⇒ To be received : 2× HERA clock

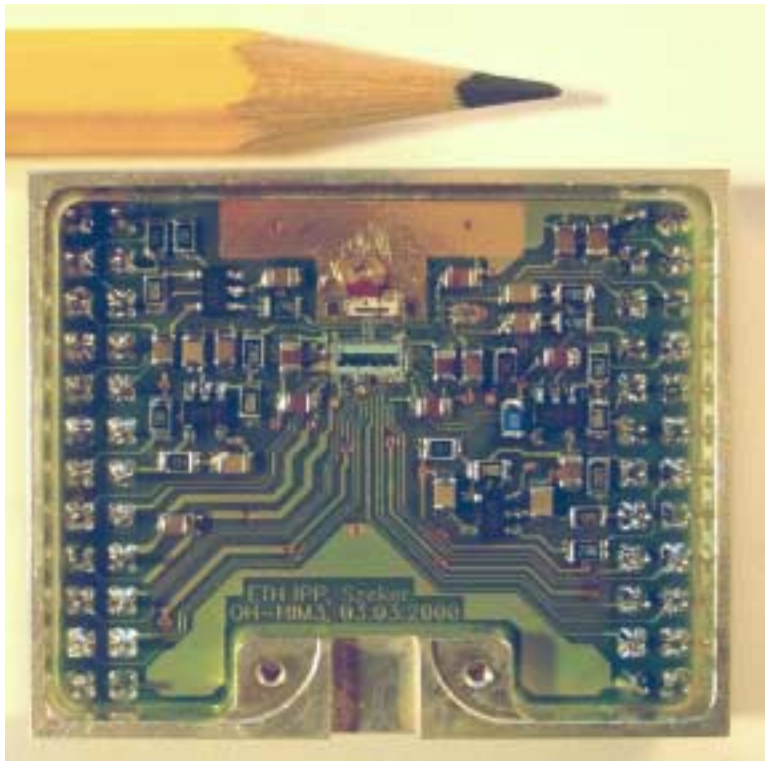
Design : Frontend–Electronics



40 identical modules :

- Consisting of :
  Frontend–Electronics
  2× Optical Hybrids (HIM, DeHIM)
  Receiver Electronics
- One optical hybrid serves two segments, mounted on one half
- PLL and power supplies on the other
- Flexible capton–PCB to bridge the high–speed data words and clock signals from / to optical hybrid
- Size : 130 mm × 2·49 mm × 8 mm
- Power dissipation :
  10 W (CIPix idle), <20 W (expected)

Design : Optical Hybrids (HIM and DeHIM)



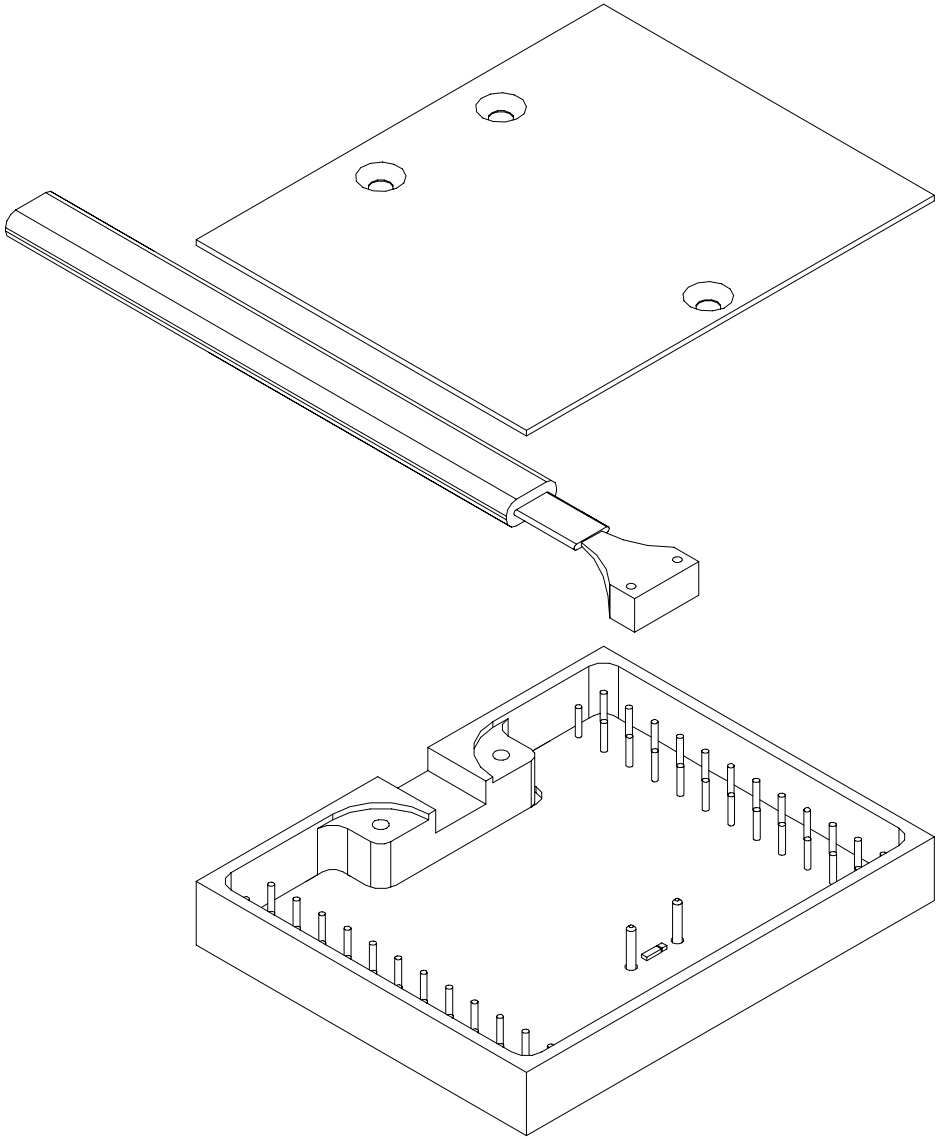
- Interface between optical and electrical regime
- Size : 410 mm × 33 mm × 6 mm
- CIP side :
  Drives data and analog channels thru VCSEL,
  receives HERA clock thru PIN diodes
  (Trigger side : vice versa)

⇒Bidirectional link
with high–speed digital–, clock– and
analog channels

Guiding pins, VCSEL and PIN must fit 250 μm pitch of MTP connectors with array of 8 fibers

⇒Alignment with 5μm precision

Design : 90° deflection

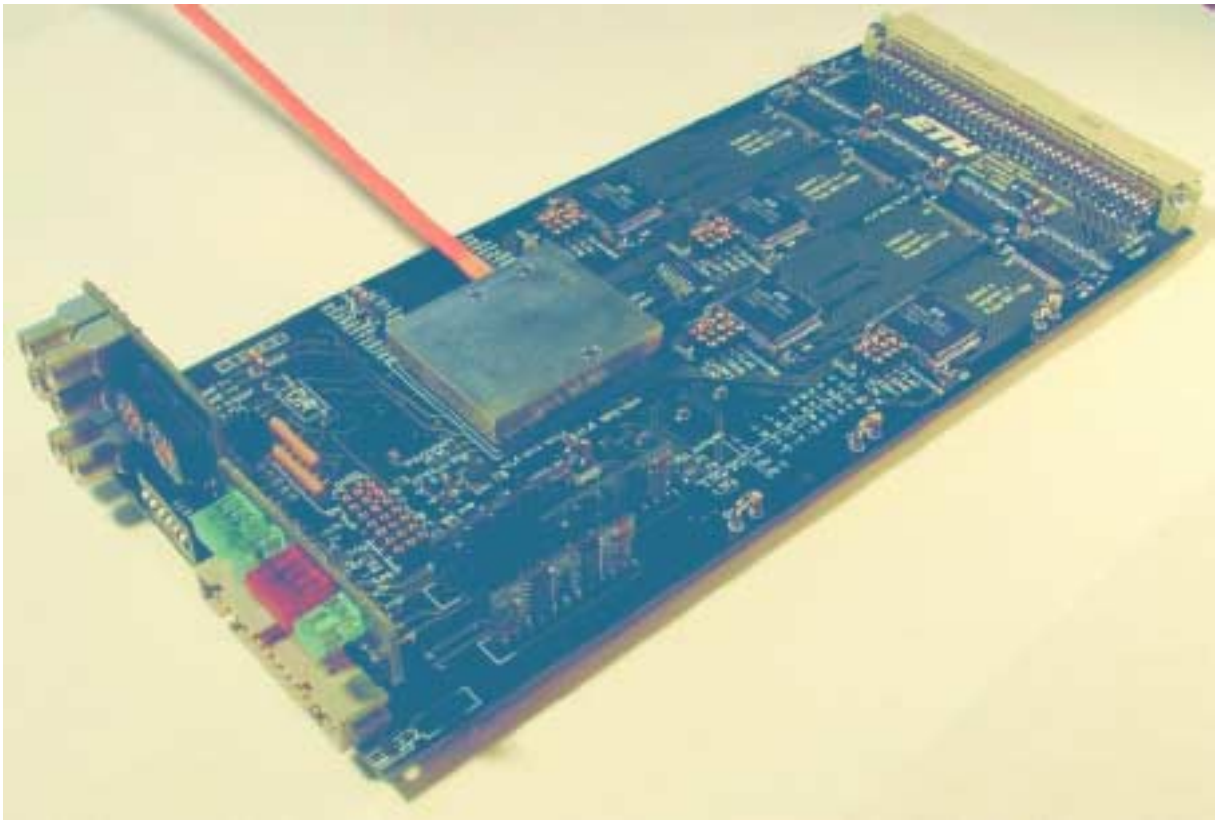


- VCSEL emit perpendicular to PCB
- Distance between two layers is $<9\,\mathrm{mm}$

  $\Rightarrow$Light needs to be deflected by 90° !
- Dismanteling MTP connector to its core (ferrule)
- Bending fibers within 2 mm height
- Using special glue to fix fibers
- Al casing gives proper mechanical connection to 90° tail.

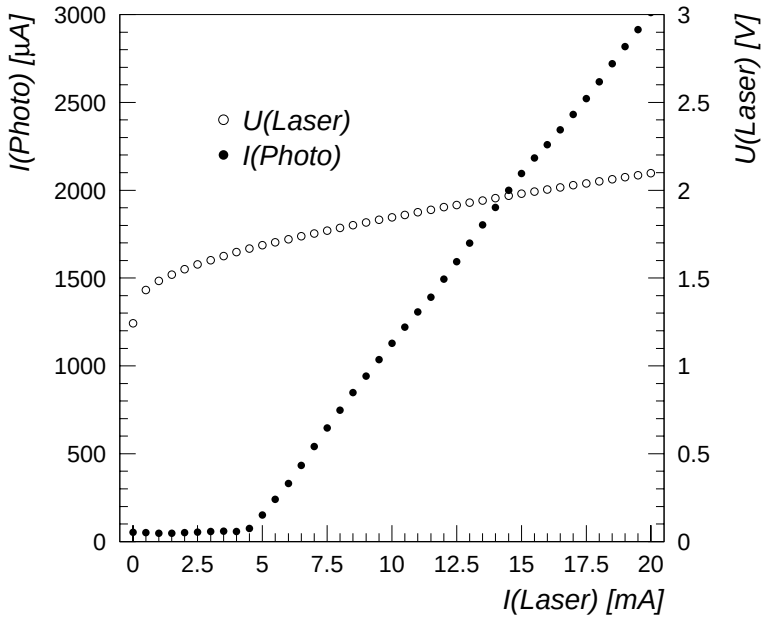
Design : Receiver Electronics

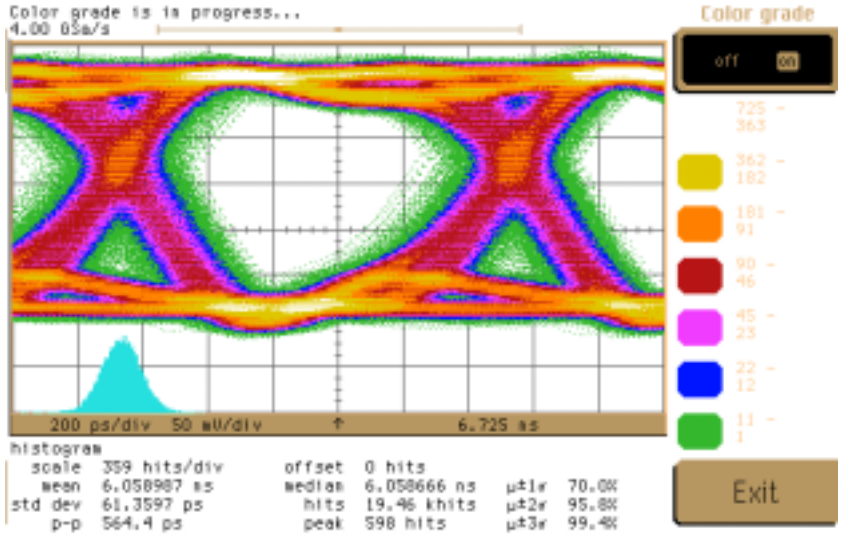
After
60 cm + 310 cm +
36 m + 30 cm
optical fibers :



- Demultiplexes and synchronizes 4×16 bit (trigger word and first word tag) and provides them for the trigger electronics
- Allows to monitor e.g. analog signals
- Provides HERA clock for the frontend electronics

Performance

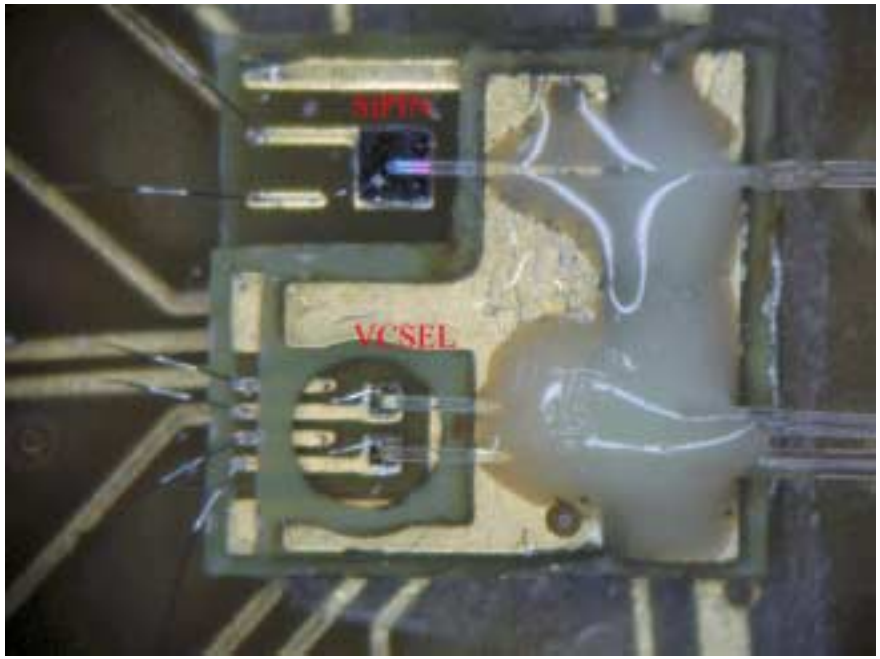




- Module protoype running stand–alone since November 1999
- VCSEL current adjusted for maximum output ⇒ Dynamic range : -3.6 ± 0.8 dBm (logical "high") -49.1 ± 4.5 dBm (logical "low")
- Crosstalk : > 20 dB
- Jitter of data word / HERA clock : < 65 ps
- Delay time : 230 ns (200 ns cables)
- Bit–Error–Rate : $< 10^{-14}$
- Test in 0..2 T magnetic field passed

⇒Prototype fullfills specifications

Optical Links for LHC Experiments



ATLAS Semi–conductor Tracker :

- 4098 modules ($6 \cdot 10^6$ strips) at 40 MHz
- Incoupling within 1.5 mm height
  a. via Si–mirror ($\epsilon = 61\%$),
  b. via 45° polished fibers
- Bit–error–rate $< 10^{-9}$
- No crosstalk seen

More optical links used by ATLAS :

- Pixel : 2500 modules ($> 10^8$ ch.) at 40 / 80 MHz, TRT : 420 000 ch. at 40 MHz, CSC : trigger with 80 $\times$ 640 Mbps uplinks and 40 $\times$ 800 Mbps downlinks, LAr : 1600 links with 32 bit at 40 MHz using HP HDMP–1022/24 or 32 bit at 77 MHz using TriQuint serializer

$\Rightarrow$ In total 45 000 frontend links

Optical Links for LHC Experiments

CMS :

- Optical links are "2nd major cost driver"
- 50 000 analog links at 40 Mbps,
  10 000 digital links at 40 MHz
- Modifying commercial multifiber solution "Paroli"

LHCb : 2000 optical links

LHC experiments using :

⇒ Single fibers at frontend, multifiber arrays at receiver side

⇒ Up– and downlinks separately, digital and analog signals separately

⇒ Radiation hard components

Conclusions and Outlook

- Complexity underestimated at the beginning :

  Optical transmission at high–speed indeed delicate; spatial constraints killed many ideas

- Multiplexer, VCSEL and fibers have just become technical "state–of–the–art"

But :

- Feasability and stability has been shown (so far) $\surd$
- Competitive to LHC experiments (exept radiation hardness) $\surd$

Nevertheless : Critical path not finished yet

- Rigid–flex–PCB : shorts between lines and vias due to misaligned capton layer **!**
- Schedule is getting tight **!**
- 90° tails and VCSEL : Long–term stability only guaranteed (not tested) **!**
- Performance of the whole system (40 modules) unknown **!**

(-; NO PAIN — NO GAIN ;-)