A Fast Track Trigger (FTT) for H1 at HERA (DESY)

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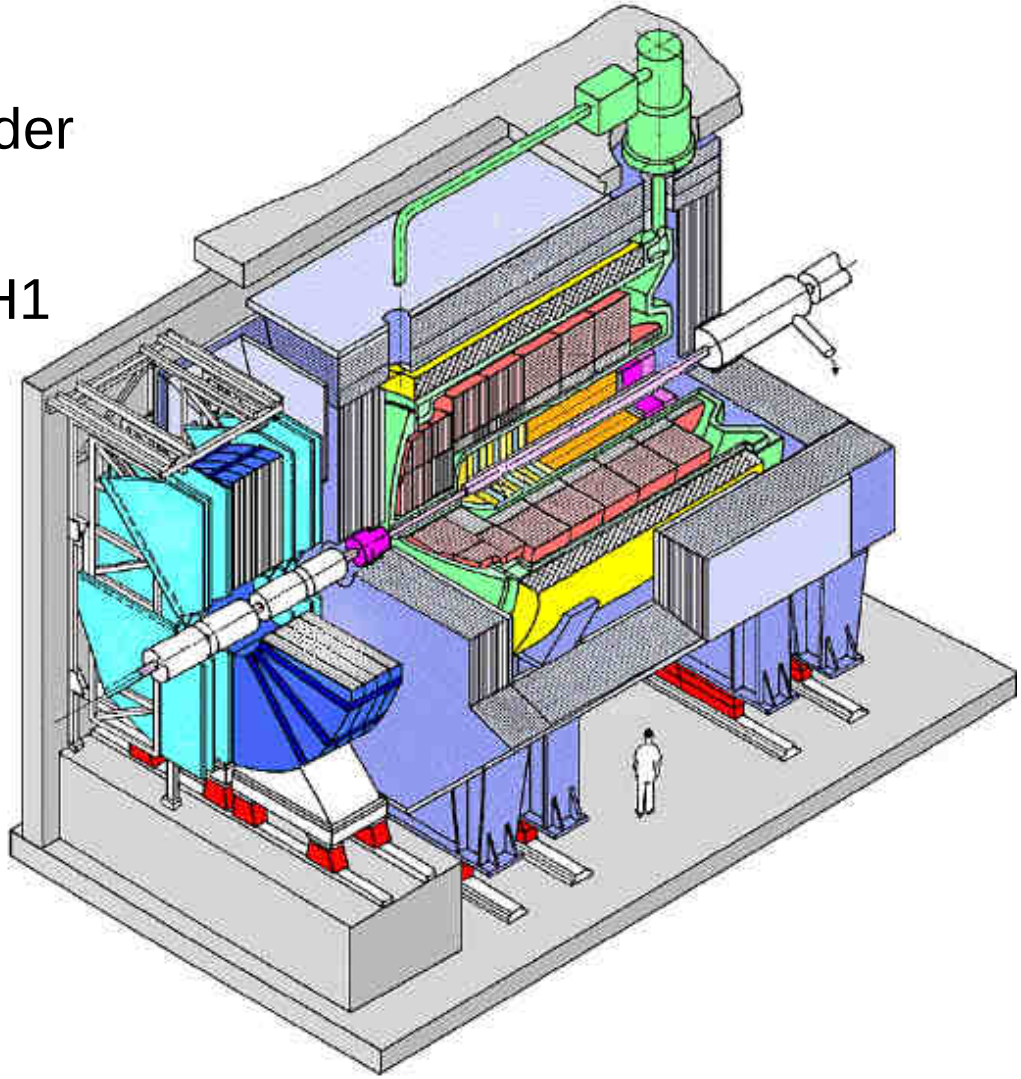
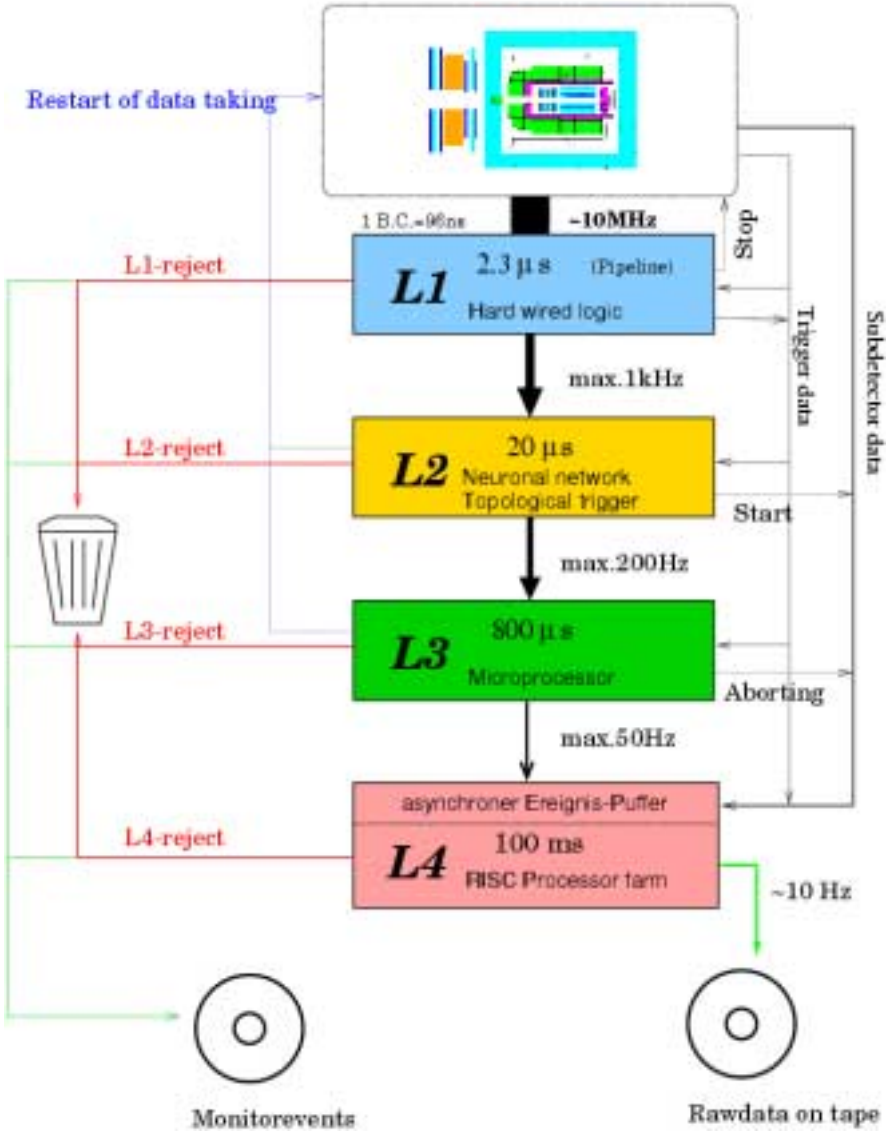
Overview: Detector

- HERA:
  $e^{\pm}$ (30 GeV) p^{+} (820 GEV) collider
  $\sqrt{s} = 320\,\mathrm{GeV}$
- Main detector components of H1
  - tracking chambers
  - Calorimeters (el., hadronic)
  - muon chambers
- Shutdown in september 2000 for luminosity upgrade
- Opportunity to upgrade detector (~18 projects)



Overview: Trigger



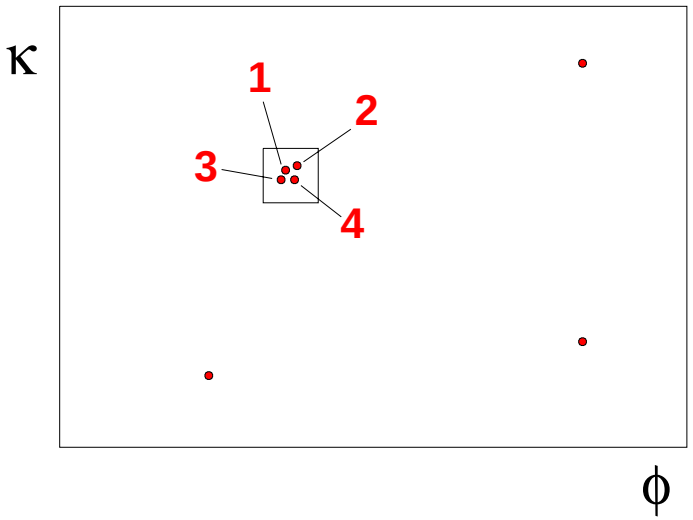
- L3 was not enabled
- Exclusive final state reconstuction only at L4
- luminosity increase about factor 5
- Downscaling with prescale factors

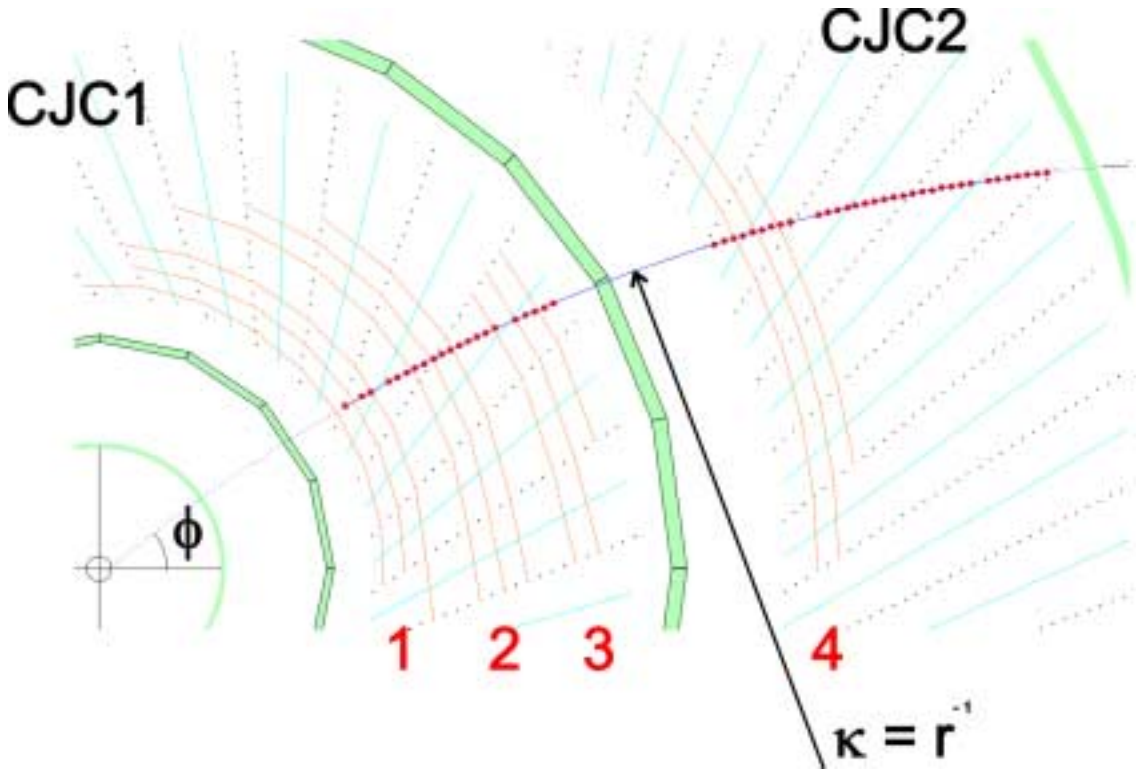
Q^2	Prescale		efficiency
	today	2001	
5	5	25	4 %
50	2	10	10 %
150	1	1	100 %

=> A fast track trigger

Concept of the FTT

- FTT in parallel to existing trigger
- FTT is based on a subset of CJC wires
- 4 layers groups with 3 wires each





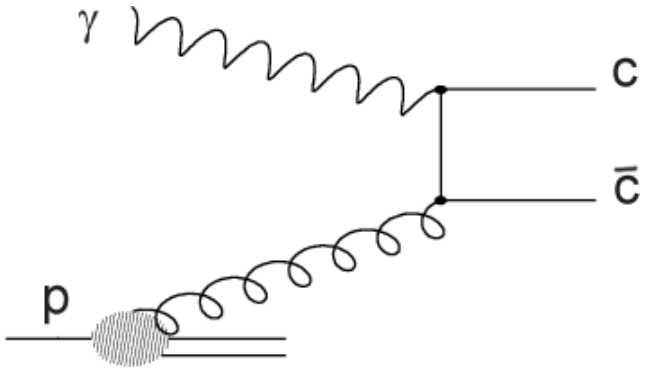
- 2d linking in κ–ϕ plane
- refit track parameters and take trigger decision

Trigger levels on FTT

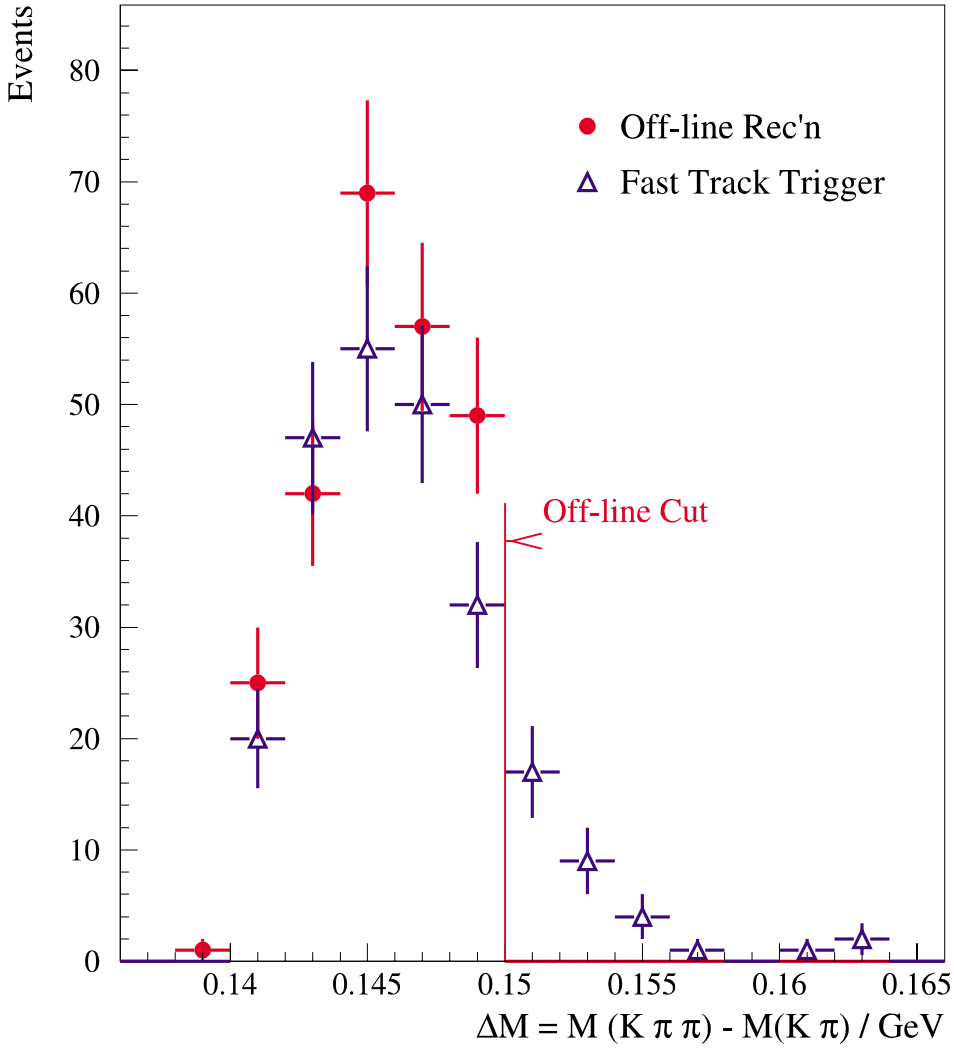
	L1	L2	L3
Latency	2.3 μs	25 μs	≈ 100 μs
Tasks	Q−t analysis, track segment finding	linking of track segments	event reconstruction
Data used for trigger	coarsely linked track segment	measured tracks	combination of tracks
Trigger decision on	p_T thresholds multiplicity charges	full track information	invariant masses, Δm

Physical Motivation

- Example:
  Measurement of gluon content of a proton in open charm production



- Identification through decay channel
  $D^* \rightarrow D^0 \pi_{slow} \rightarrow K \pi \pi_{slow}$
- Cut on $\Delta m = m(K \pi \pi_{slow}) - m(K \pi)$



Physical Benefit

Process	efficiency FTT [%]	efficiency prescale [%]
D^* decay (DIS)	70	1
D^* decay (γp)	60	1
$\rho \rightarrow \pi^+ \pi^-$	80	2
$J/\Psi \rightarrow \mu\mu$ (ee)	60 (12)	3 (1)
$\Upsilon \rightarrow \mu\mu$ (ee)	60 (12)	3 (1)
$W \rightarrow \mu\upsilon$	70	3 (1)

- Resolution of FTT from D^* events (=> Binning of the κ–ϕ plane):

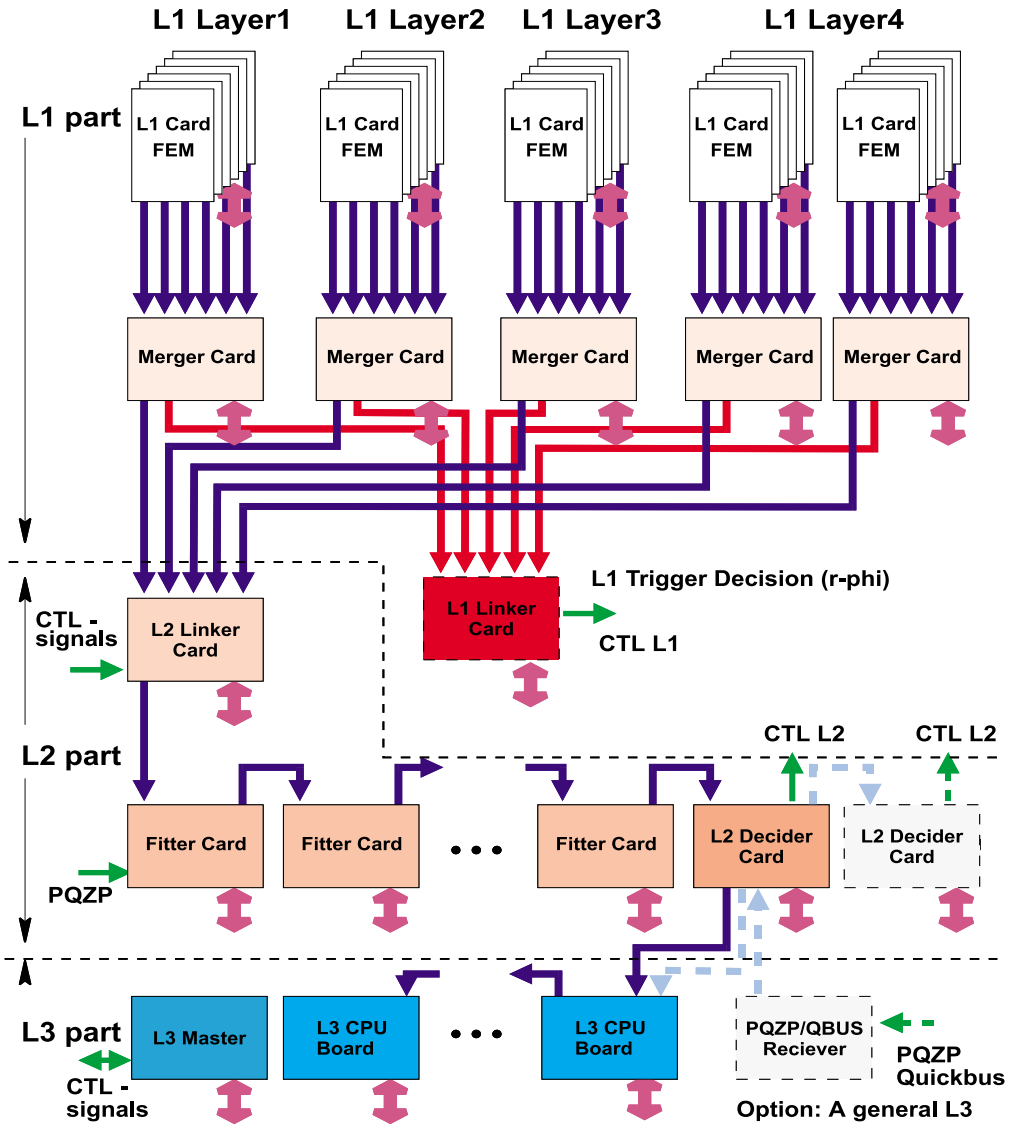
$$\sigma\left(\frac{1}{p_T}\right) = 0.04 \frac{1}{\text{GeV}} \qquad \sigma(\phi) = 6\,\text{mrad}$$

z information calculated from charge divison

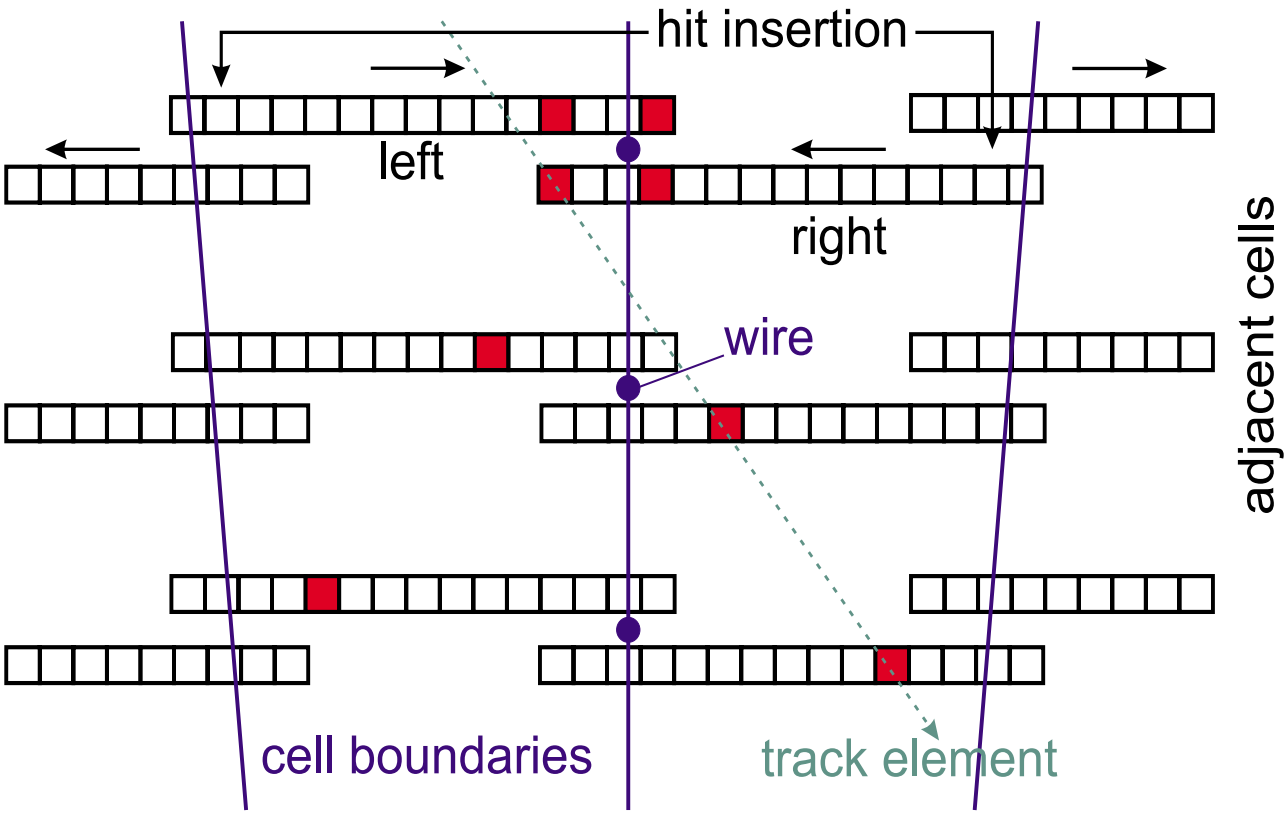
$\sigma(z) \approx 4\,\text{cm}$ => $\sigma(\theta) = 50\,\text{mrad}$

Hardware: Overview

- L1:
  - Flash ADC (80 MHz)
  - hits are filled in shift registers
  - compare hit pattern to valid masks (several 1000)
  - total 30 FEM
- L2:
  - collect all track segment
  - linking in κ–ϕ histogram
  - non iterativ circle fit on DSP
  - 1 multipurpose card
- L3:
  - commercial board with 450 MHz PowerPC750
  - 4–16 PPC

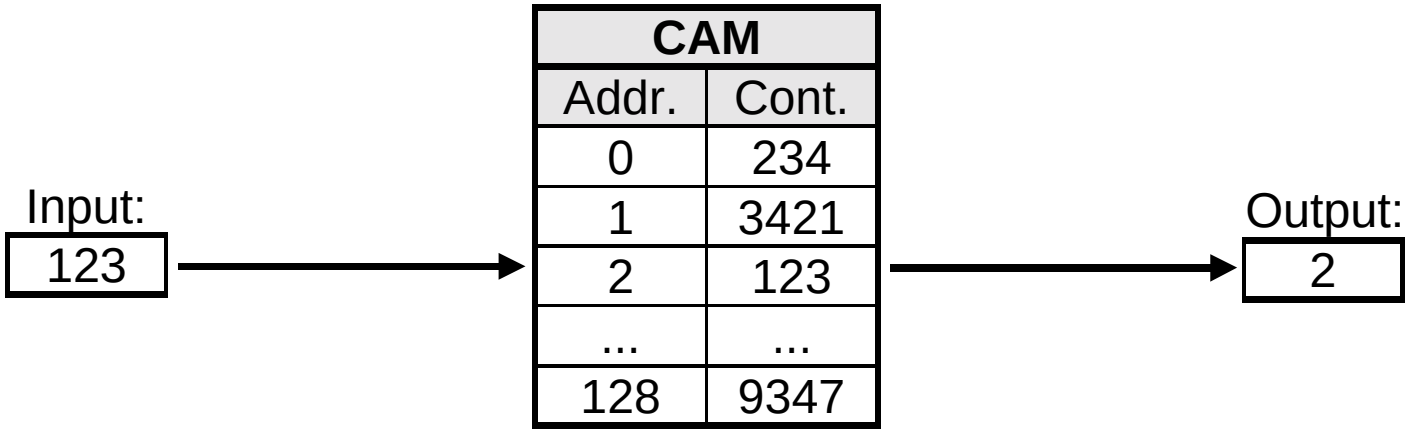


Track segment finding



Hardware: FPGA

- Modern programmable chips:
  FPGA (Field Programmable Gate Array)
- High density of gates (> 1 million)
- speed: 100 MHz or more, number of I/O pins > 400
- Programmed logic can be modified any time (via VME)
- Key technique for FTT:
  CAM (Content addressable memory)



Hardware: Development

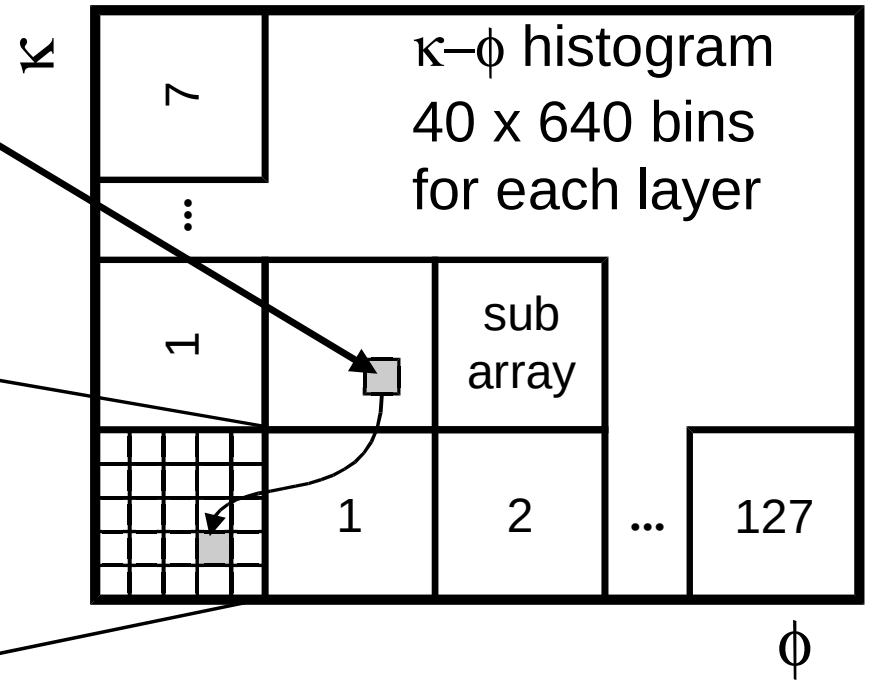
- Institutes involved in the project:

L1	Rutherford Appleton Lab
	Uni of Manchester
	Uni of Birmingham
L2	Supercomputing Systems (SCS)
	ETH Zürich
	Uni Dortmund
L3	Uni Dortmund

- Development status:
  - feasibility has been shown
  - hardware is in design stage

L2 linking: κ–ϕ histogram

Input from L1:
track segment with
– bin number (κ,ϕ)
– track information



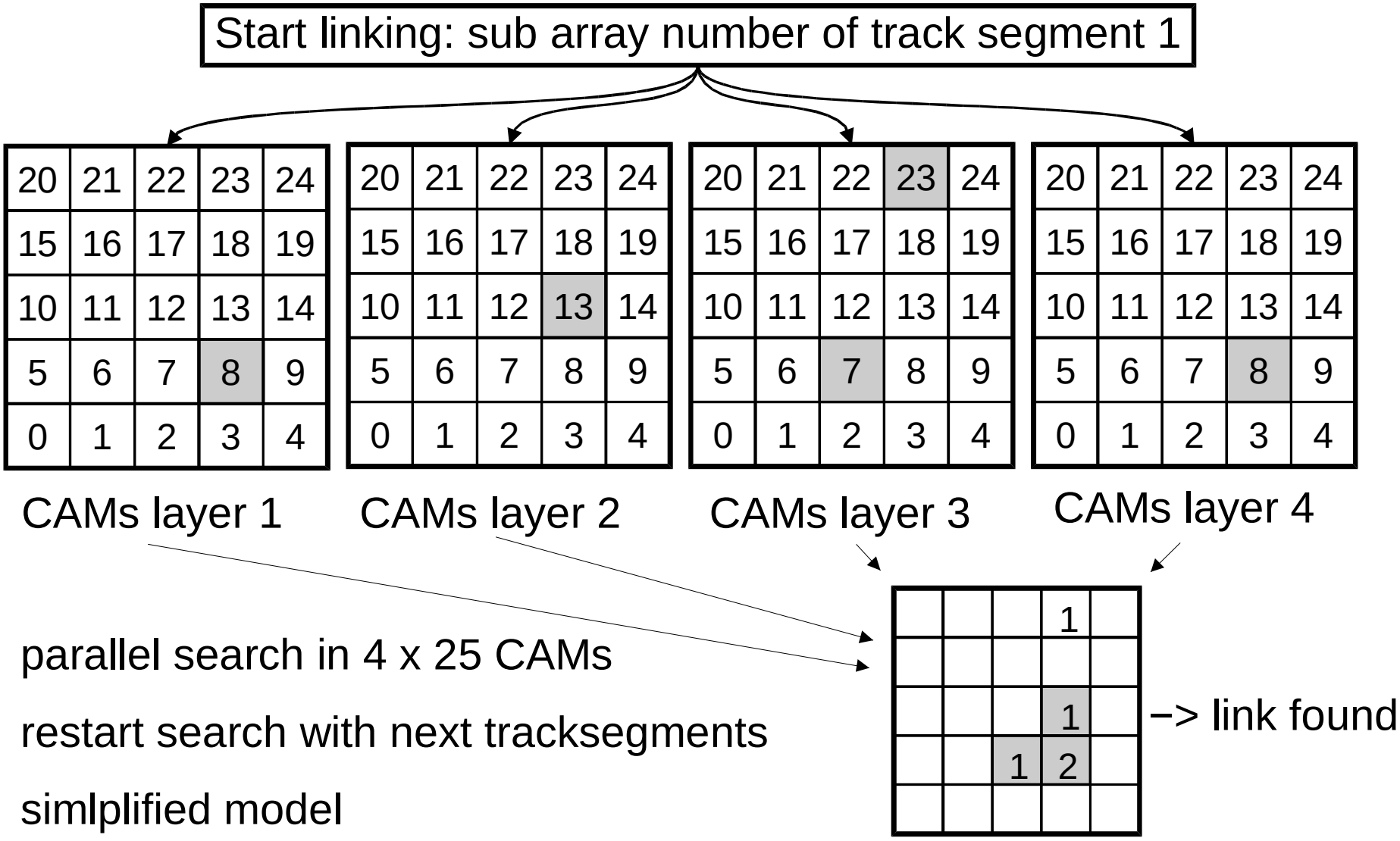
20	21	22	23	24
15	16	17	18	19
10	11	12	13	14
5	6	7	8	9
0	1	2	3	4

Matrix of 25 CAMs
for each layer
(fine binning)

CAM 8	
1	sub array number
2	...
.	...
32	...

RAM 8	
1	track information
2	...
.	...
32	...

L2 linking: link track segments



- parallel search in 4 x 25 CAMs
- restart search with next tracksegments
- simlplified model

Summary

- Exclusive track based triggering is necessary after HERA luminosity upgrade
- FTT is a very flexibel system (hardware & trigger)
- Good integration of FTT in the existing trigger
- FTT provides L1−, L2− and L3−keep signal
- Realisation possible due to chip development of past years
- FTT is fast:
  − process 40’000 events per second
  − recunstruct 2 million tracks per second