Development of CMS Pixel Readout System

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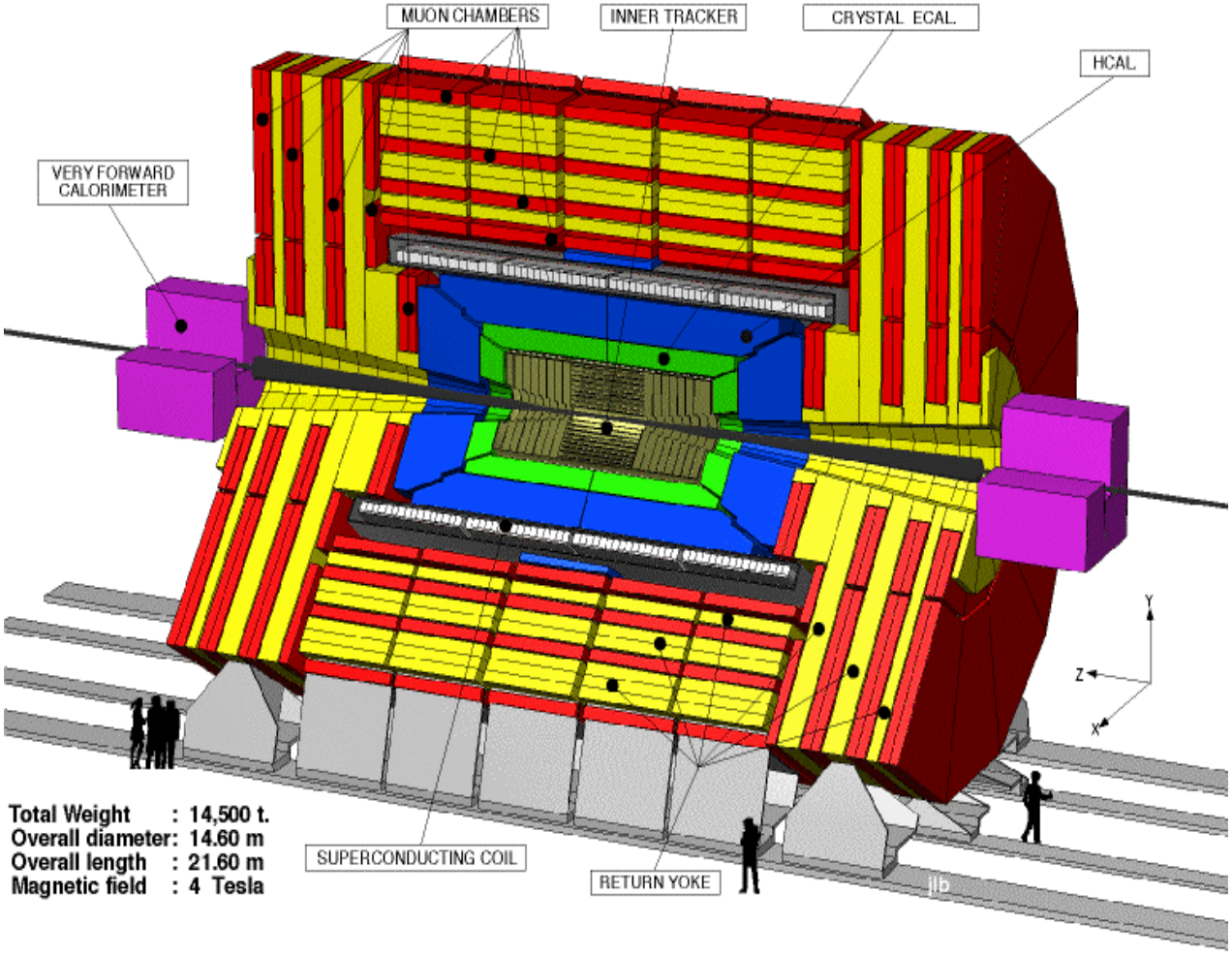
The CMS Detector



The pixel detector is the innermost part of the inner tracker system.

The Pixel Tracker System and Requirements

Why do we need the pixel detector:

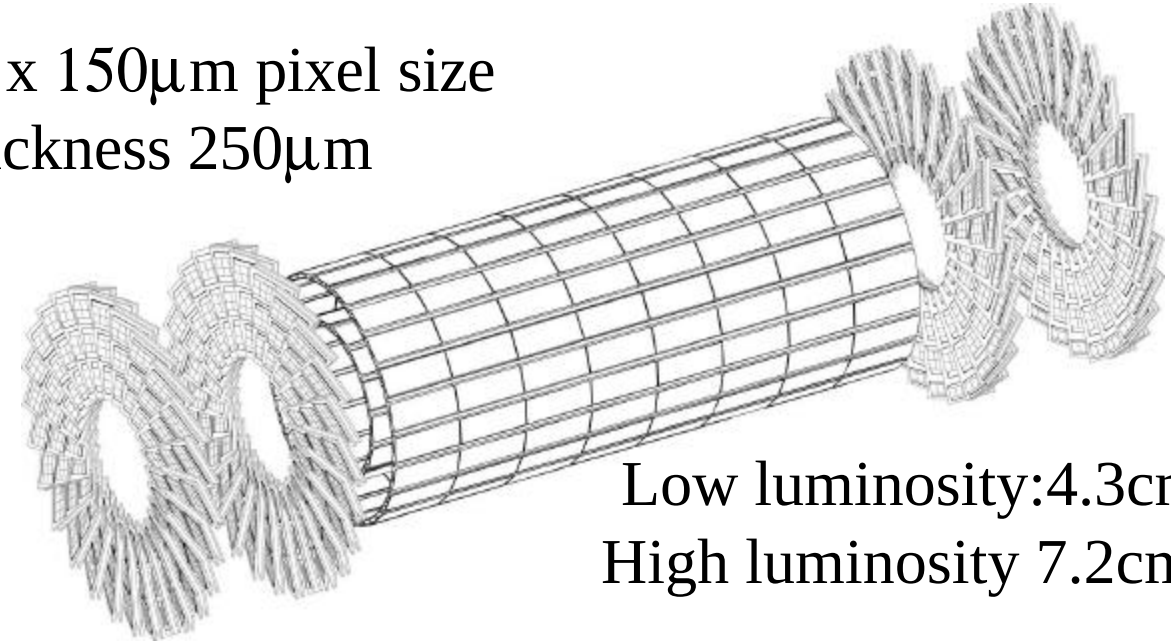
- To reconstruct primary and secondary vertices from b-jets and other objects(c , τ)
- High particles flux, MC study shows 1000 tracks per bunch crossing(25ns)
- In order to reconstruct a track we need at least two hits per track, so we need two pixel layers

What are the requirements on the pixel detector:

- The detector material must survive the of up to $6x10^{14}$ hadrons per cm^2
- The analog readout block must be able to deal with increased leakage current, reduced charge collection, with damage to the circuit itself
- The front-end readout architecture must operate with good efficiency in spite of high hit and trigger rates

The Pixel Detector

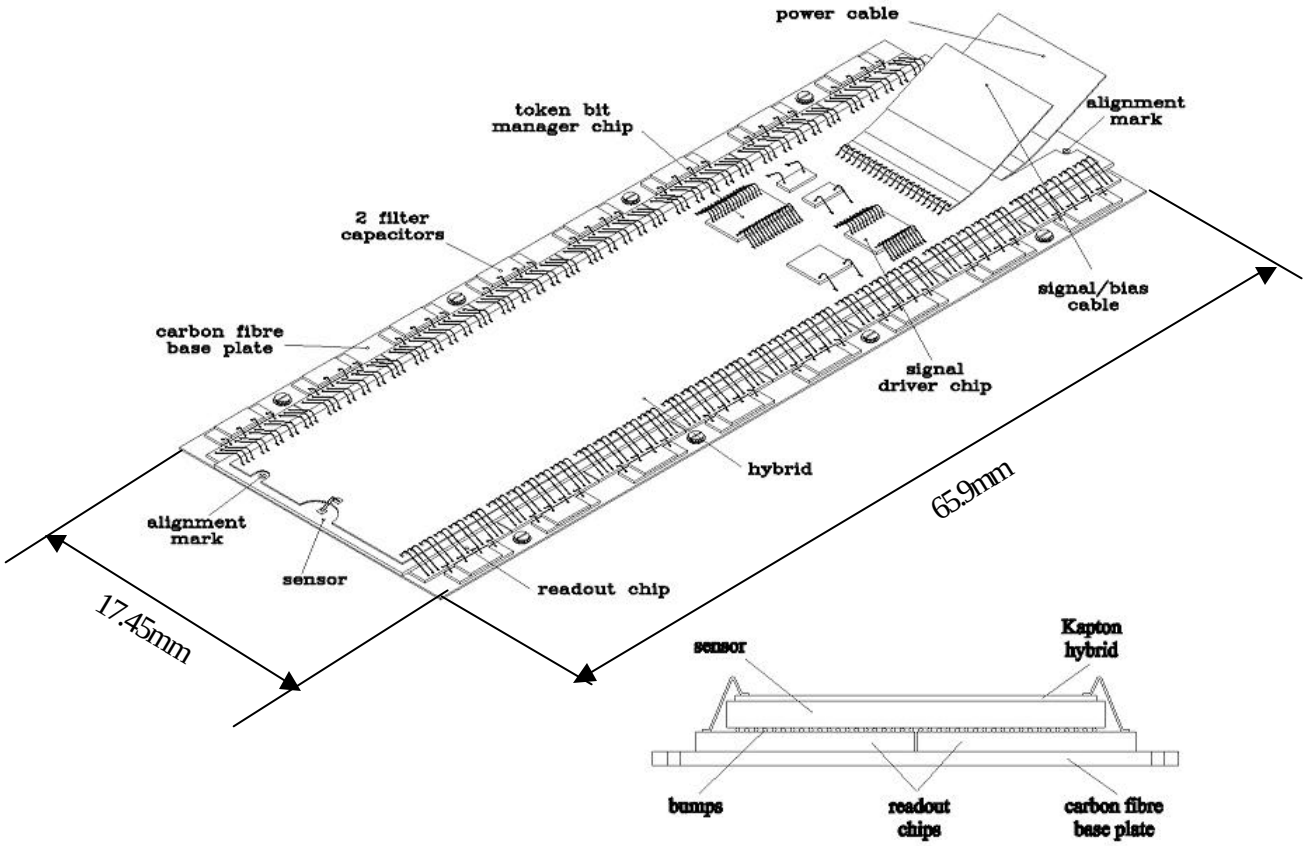
150µm x 150µm pixel size
thickness 250µm



Low luminosity:4.3cm and 7.2cm
High luminosity 7.2cm and 11.0cm

- The whole pixel system consists of about 800 detector modules
- The total amount of the readout chips is about 12000
- Each readout chip (ROC) reads 53*52 pixels
- Single pixel counting rate will be about 10kHz
- Estimated resolution is about 15µm

The Pixel Detector Module



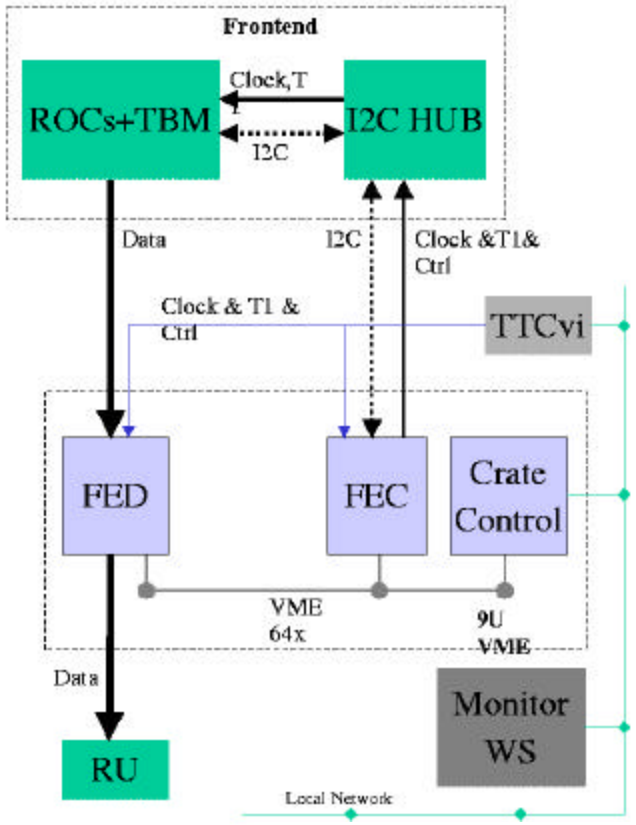
General Overview of the Pixel Detector Readout

Front-end part:

- Silicon sensor
- Readout chip
- Token Bit Manager
- Interface to controlling signals

Readout part:

- Front End Controller
- Front End Driver
- Interface to monitoring Workstation



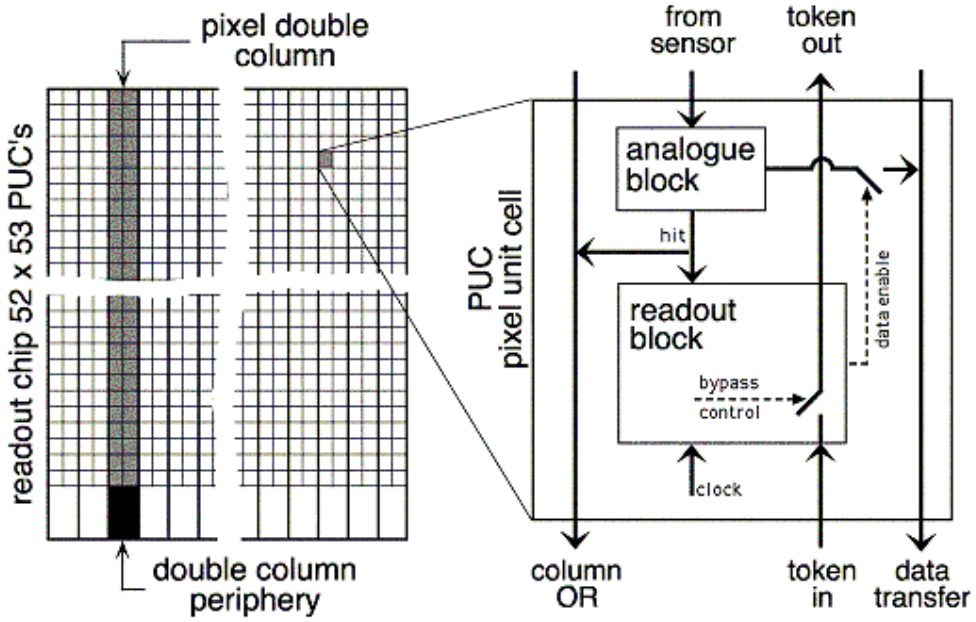
Purposes of My Research

My plans for 2001 year and for the next few years:

- To measure the influence of the leakage current of the pixel on the analog block, delays in the analog block
- To take part in the development of the prototype of the pixel detector
- To measure different properties of the prototype at CERN test beam, such as charge collection, noise, spatial resolution, radiation hardness
- To take part in the development and construction of the digital readout of the pixel detector and measure it's performance, track reconstruction efficiency, using the prototype of the pixel detector

I'll show some measurements I have done for different variants(#2 and #4) of the analog block of the readout chip "PSI41" in order to optimize parameters of the circuit.

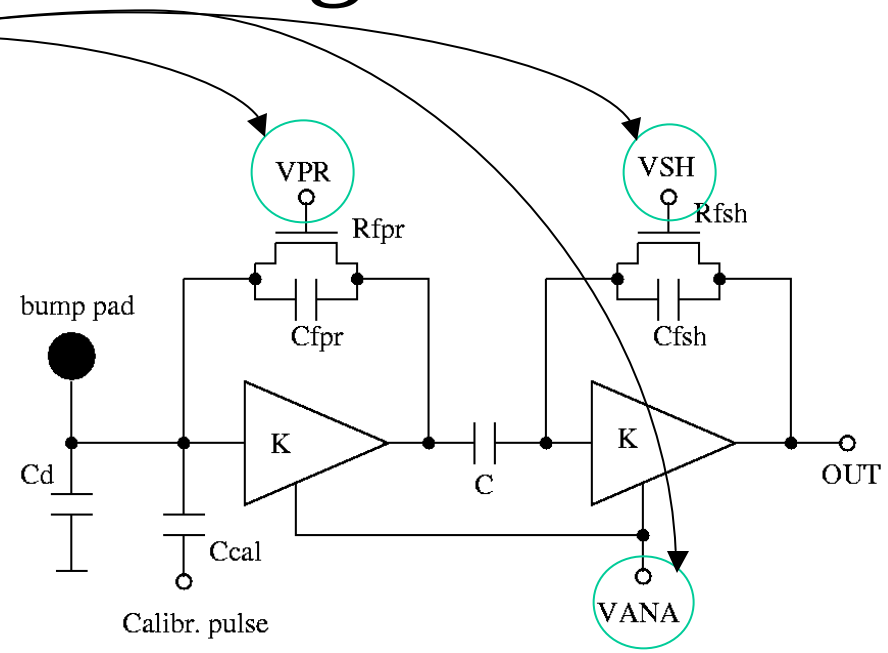
The Pixel Unit Cell



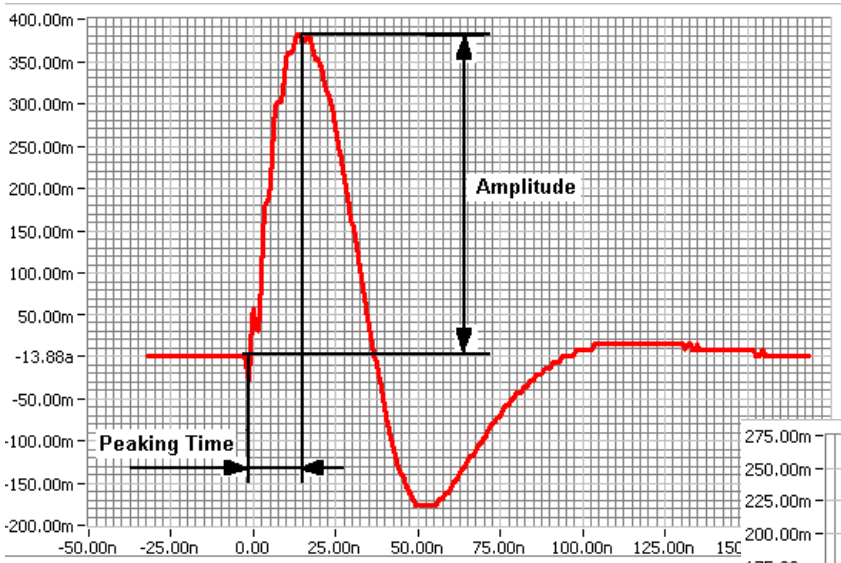
Each sensor pixel connected via bump bond to its own readout circuit on the readout chip, which is called Pixel Unit Cell (PUC). The analog block is used to amplify the signal from the pixel.

Test of the Analog Block

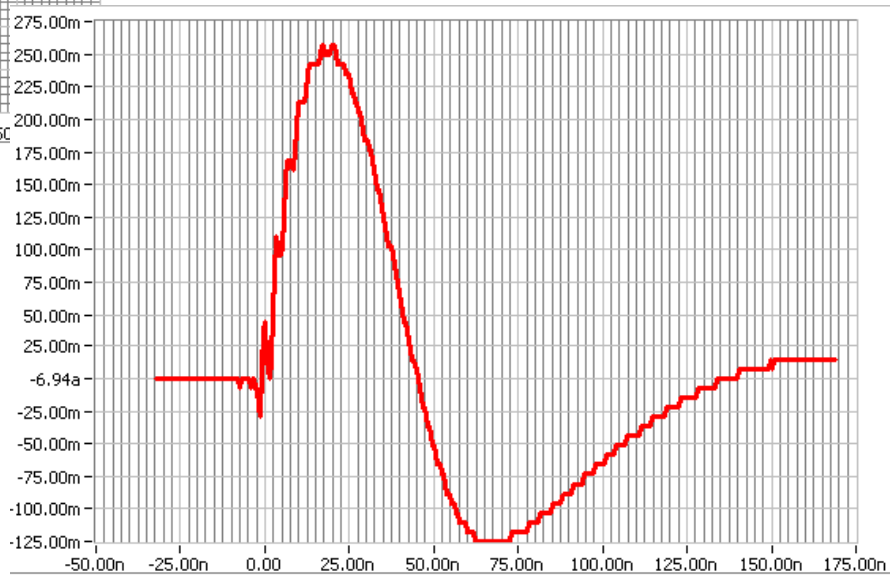
- I have three dimensional parameters space: VPR,VSH,VANA which were varying in some range
- All measurements were done for #2 and #4 of PSI41 readout chip
- The detector capacitance can be disconnected from the input and properties measured without it
- The measured parameters are: power consumption, gain and peaking time



Test of the Analog Block

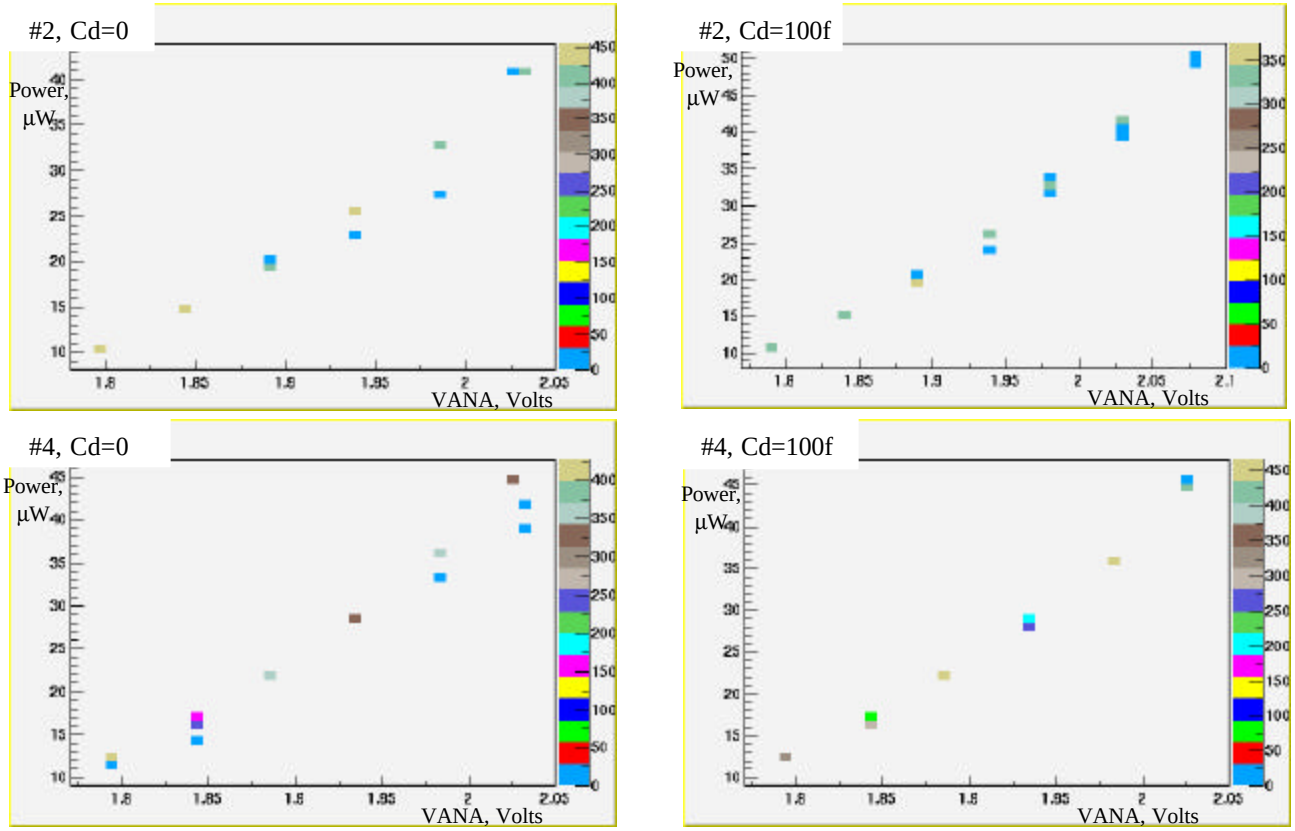


Typical waveforms for PSI41#4 for detector capacitances 0(top) and 100fF(bottom). The input charge is 10000e, VPR=2.6V, VSH=2.67V, VANA=2.01V, Power=41.4µW



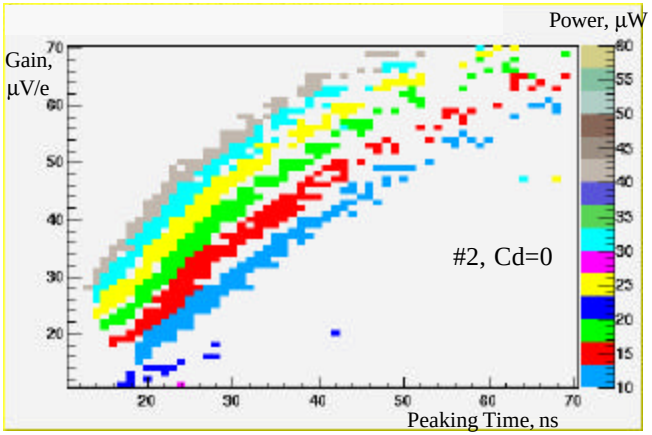
Gain is defined as the ratio of Amplitude to the input injected charge

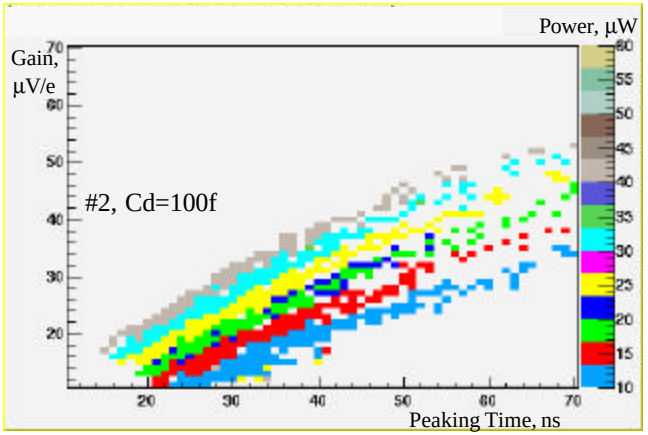
Test of the Analog Block

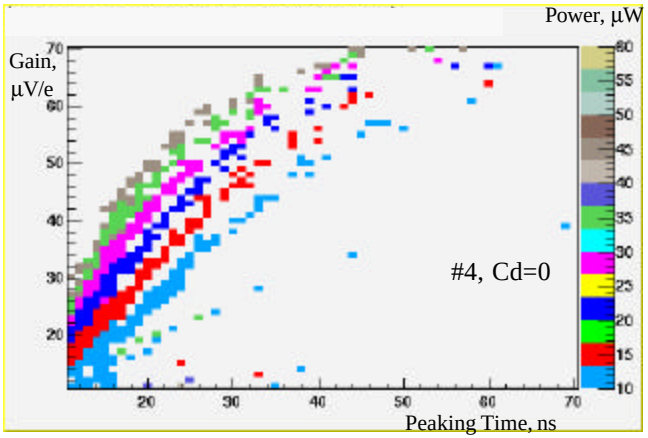


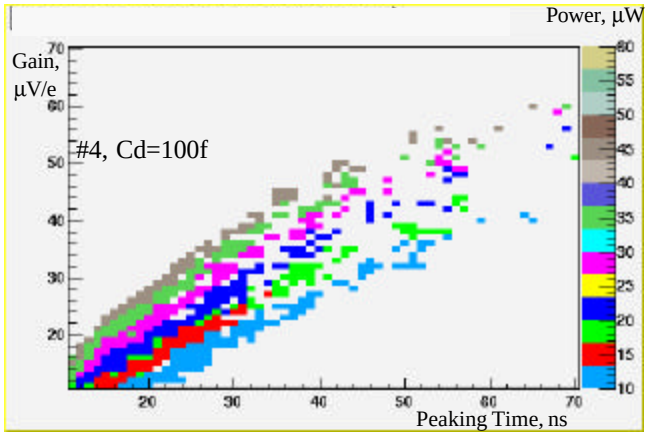
Distributions of the power versus parameter VANA. From the correlations one can conclude that power consumption mainly depends on analog voltage (VANA).

Test of the Analog Block



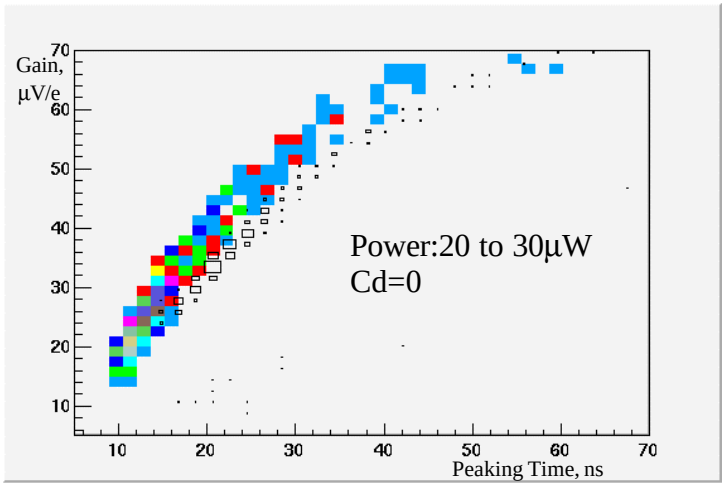


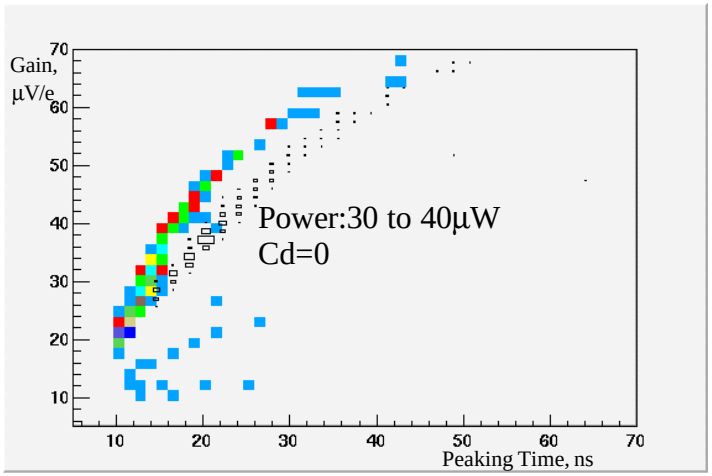


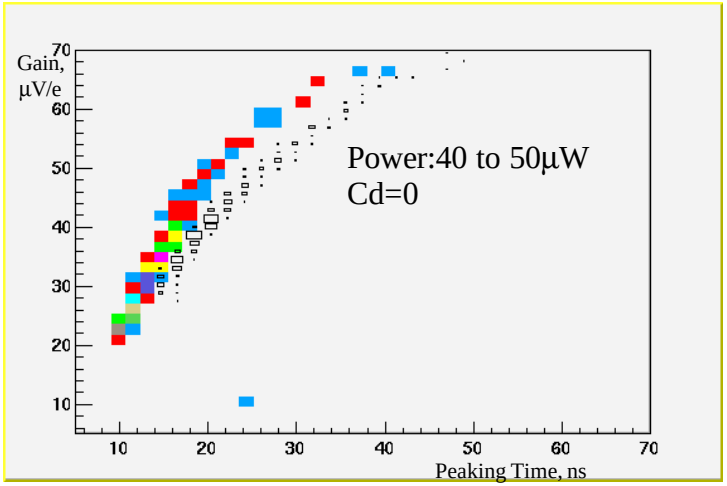


Different points in the parameters space(VPR,VSH,VANA) may lead to approximately the same gain and peaking time. In every unit cell(1µV/e*1ns) in the two dimensional space of the Gain (in 1µV/e) and the Peaking Time(ns) the minimum power(µW) was found and this value is plotted as a function of two variables. From this we can see that when the detector capacitance is connected to the input, the gain decreases and peaking time increases for the same power consumption.

Test of the Analog Block

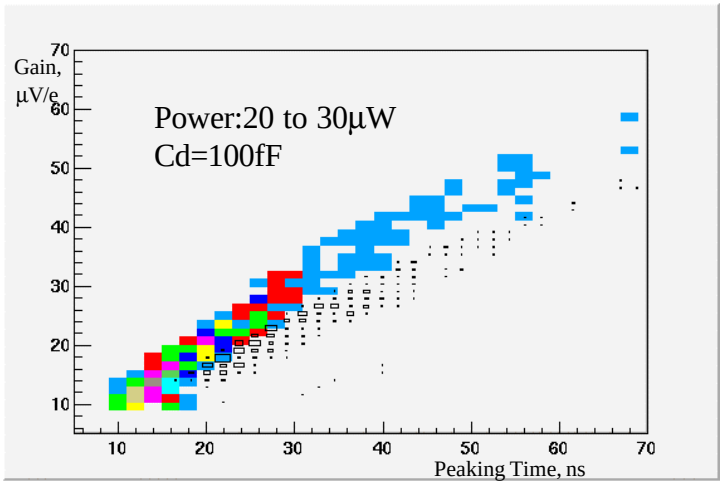


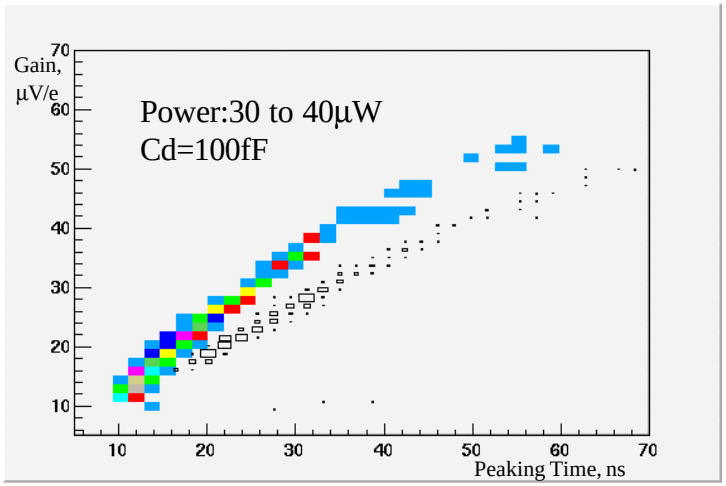


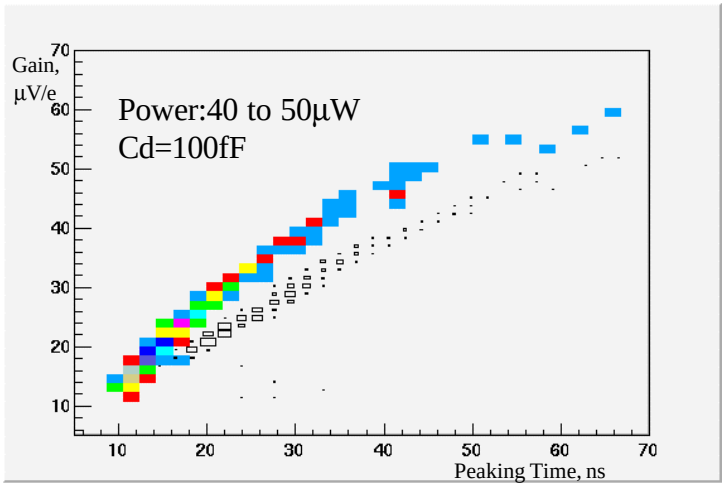


Histogram(events are different parameters setting) where Y is the output Gain (in μV/e) and X is the Peaking Time(ns). Color squares for #4, boxes for #2 variants of “PSI41” chip. One can see that #4 is better, because it has a higher Gain at the same peaking time and power consumption.

Test of the Analog Block

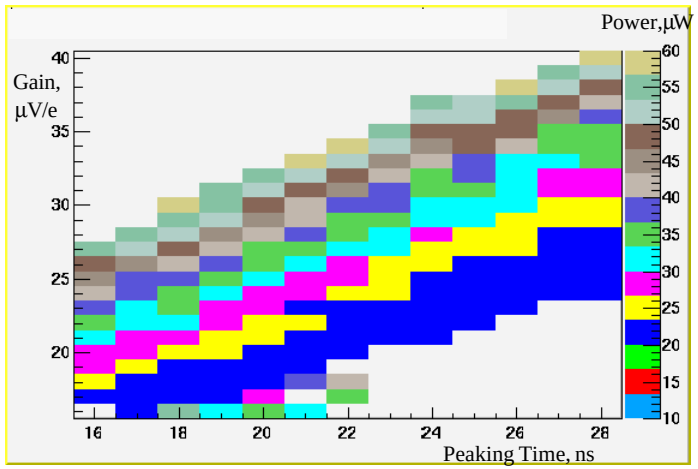


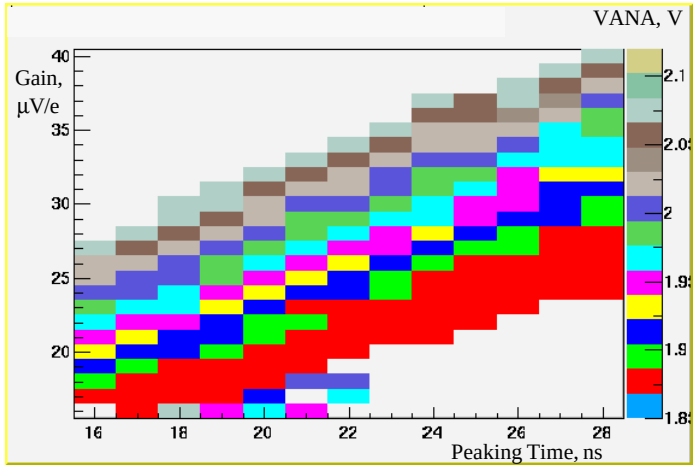


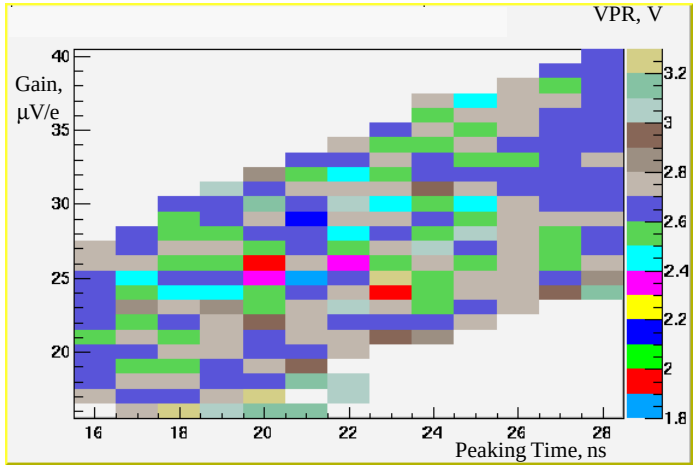


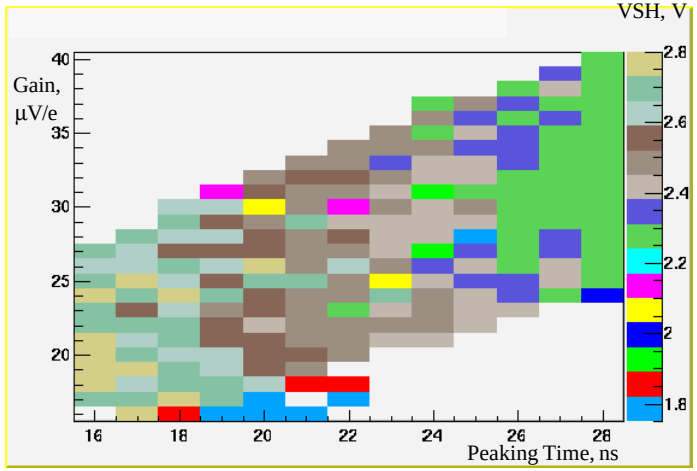
The similar plots as previous, but with detector capacitance connected to the input.Color squares for #4, boxes for #2 variants of “PSI41” chip. Again #4 is better.

Test of the Analog Block









Measurements for #4 of “PSI41” chip with detector capacitance at the input. In every unit cell(1µV/e*1ns) in the two dimensional space of the Gain (in 1µV/e) and the Peaking Time (ns) the minimum power(µW) was found and this value is plotted as a function of two variables(top left). Next three plots show three parameters VANA, VPR and VSH in the same coordinates and at which the minimum power was found.

Conclusions

The version #4 of readout chip(PSI41) looks very attractive in comparison to version #2 because:

- It has for the same peaking time and power the higher gain.
- For the same peaking time and gain it has lower power consumption which is very important, for example decreasing even 1uW in power will lead to decrease the total power by about 50Watt due to the fact that the number of pixels is very large ~50 millions. The decreasing of the power will decrease the material budget for power supply and cooling.