The Read Out Chip of the CMS Pixel Detector

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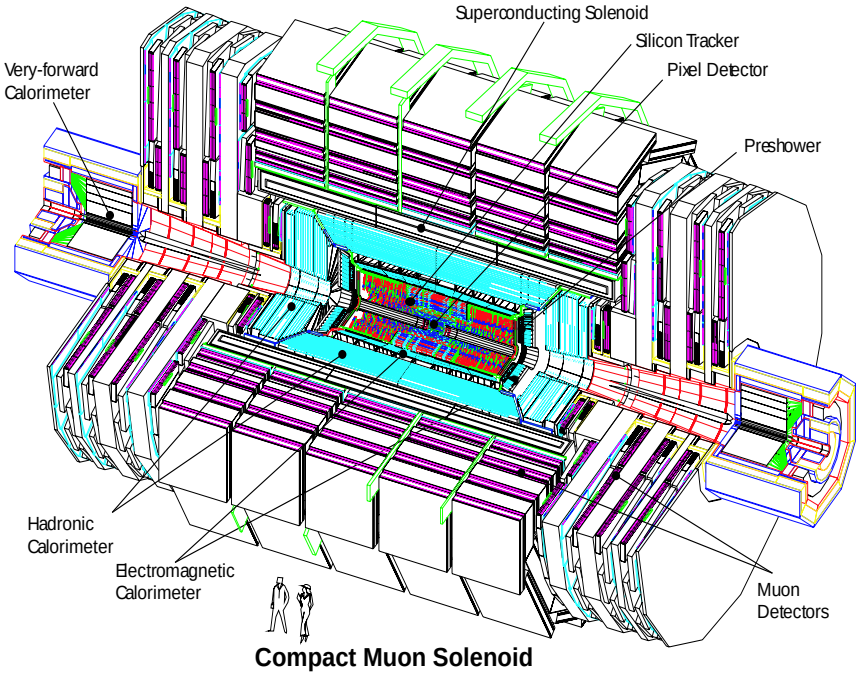
PSI

- **CMS Pixel Detector**
- **PSI46**
- **Testbeam 2003**



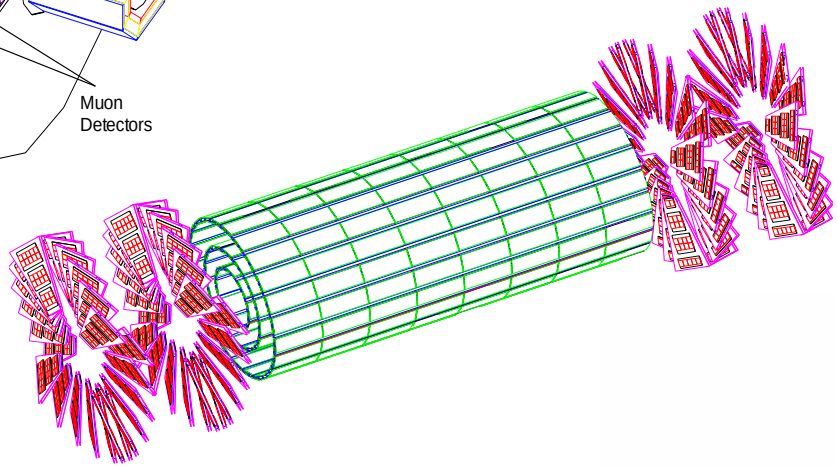
CMS detector

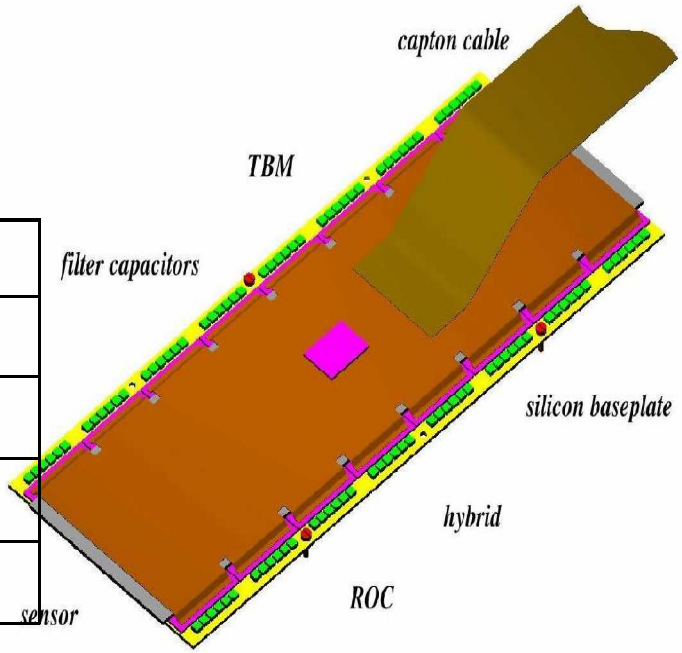
innermost tracking detector

CMS pixel detector

basic building block

pixel module





Layer	Radius	# Modules	# Chips	# Pixels	Area
	[cm]			[$\times 10^6$]	[m^2]
1	4	128	2`304	9.6	0.15
2	7	224	3`840	16	0.25
3	11	320	5`376	22.4	0.35

LHC environment:

- **40 MHz bunch crossing frequency**
- **50 kHz Level 1 trigger rate**
- **fluence up to 50 MHz/cm^2**

requirements on Read Out Chip (ROC):

- **register pixel addresses and bunch crossing numbers**
- **zero-suppression**
- **data taking and simultaneous readout operation**
- **radiation hard design**
- **low power consumption**
- **analog pulse-height information**

Development of the CMS pixel read out chip

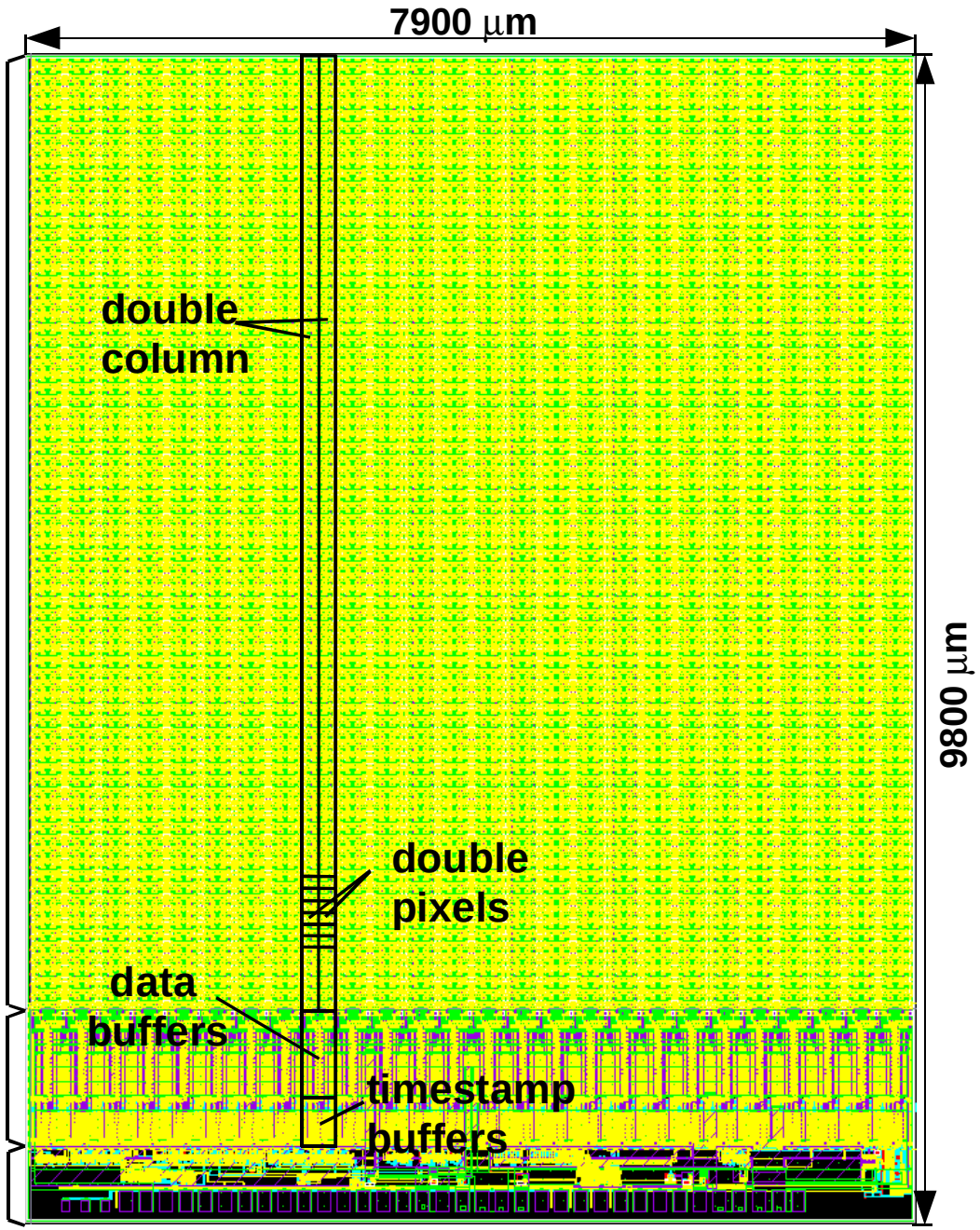
- **development started in DMILL technology**
  - **radiation hard technology**
  - **0.8 μm, two metal layers**
    - ⇨ **design: limited # of transistors/pixel and bus lines**
    - ⇨ **PSI43 in Summer 2002: complete functionality, basically working, insufficient rate capability for high luminosity**
- **Translation to Deep Sub Micron (DSM) technology**
  - **designed radiation hard**
  - **0.25 μm, five metal layers**
  - **half voltage, half current**
  - **PSI43 translation: September 2002 ⇒ June 2003**
    - ⇨ **PSI46 received August 2003**

PSI46 overview

pixel array:
52 columns x 80 rows = 4160 pixels
(organised in 26 double columns)
pixel size: 100 μm * 150 μm

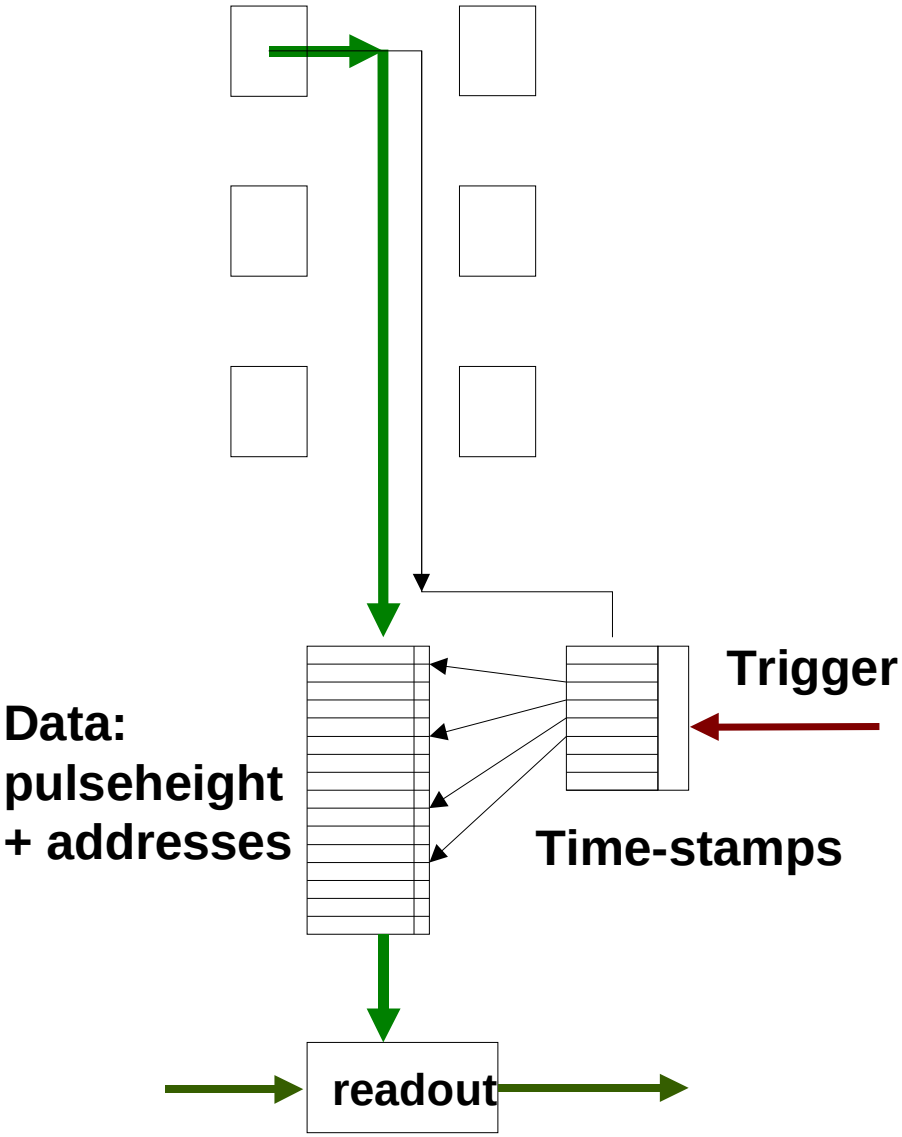
double column periphery, pixel – column interface, (32 data buffers, 12 timestamp buffers)

control interface block, I2C, DACs, regulators, counters, supply pads

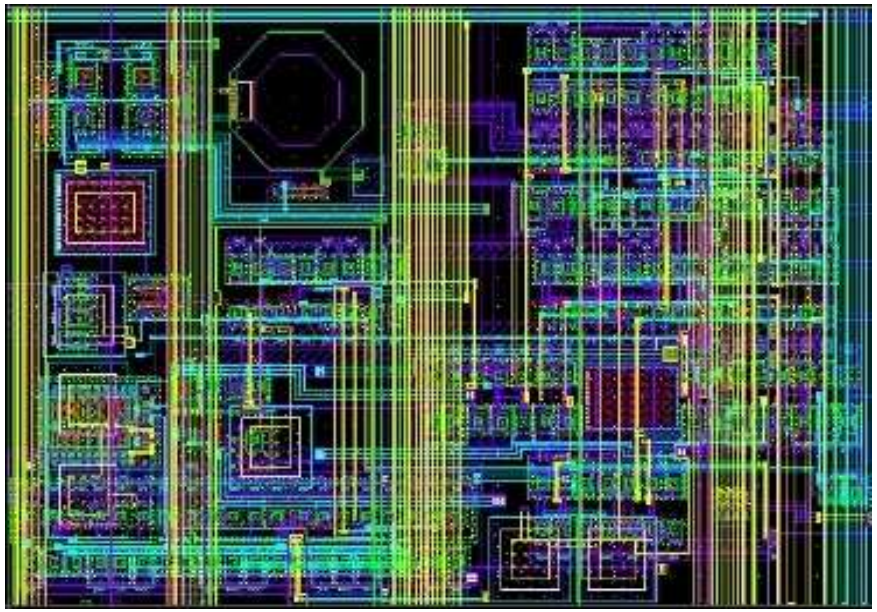


Architecture of PSI46

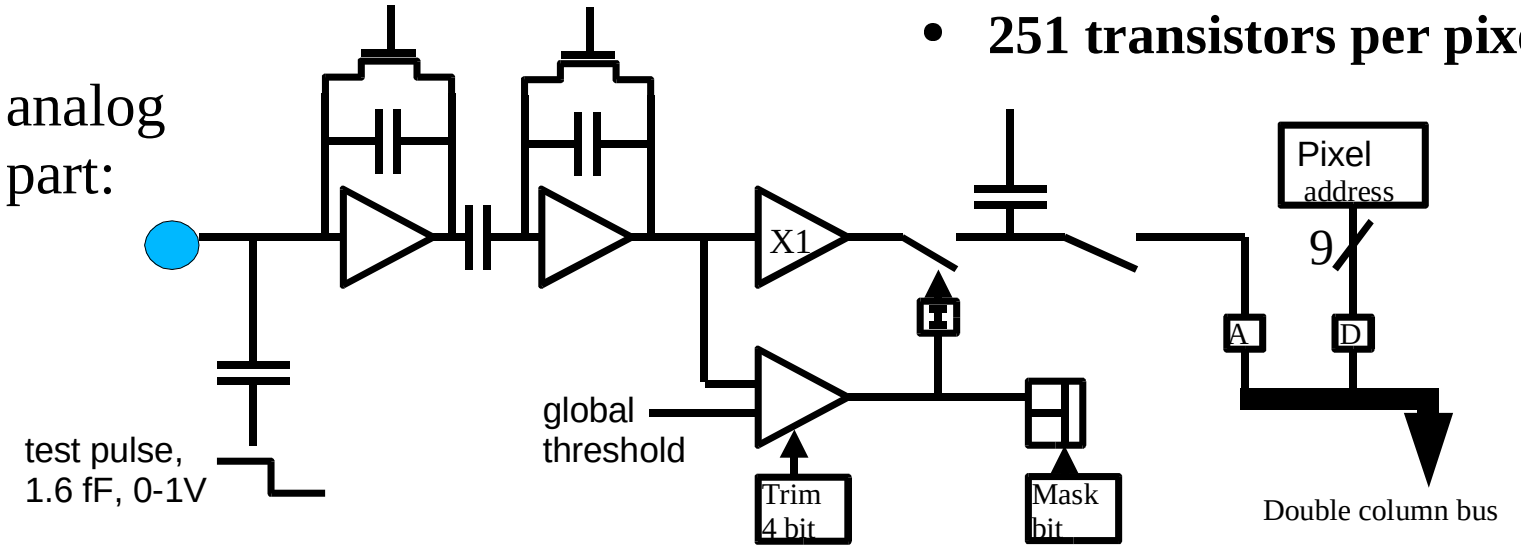
- **pixel:**
  - **no clock, counter or buffer**
  - **waits for hits, notifies periphery**
- **column periphery:**
  - **sets time-stamps**
  - **collects data from pixels, buffers data**
  - **until confirmed by the CMS trigger or latency passed**
- **readout of triggered data after token enters the chip**



Pixel Unit Cell of the PSI46



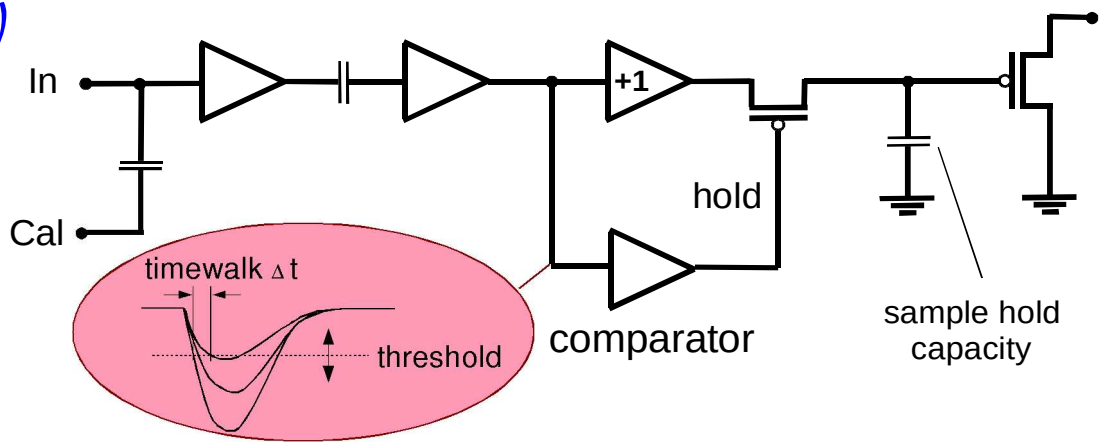
- **analog:**
  - **pre-amplifier, shaper, sample-hold mechanism, comparator**
- **threshold:**
  - **8 bits global**
  - **4 bits local trim**
- **pixel address:**
  - **9 bits digital**
- **251 transistors per pixel**



Parameters of DMILL and new DSM Pixel Read Out Chip

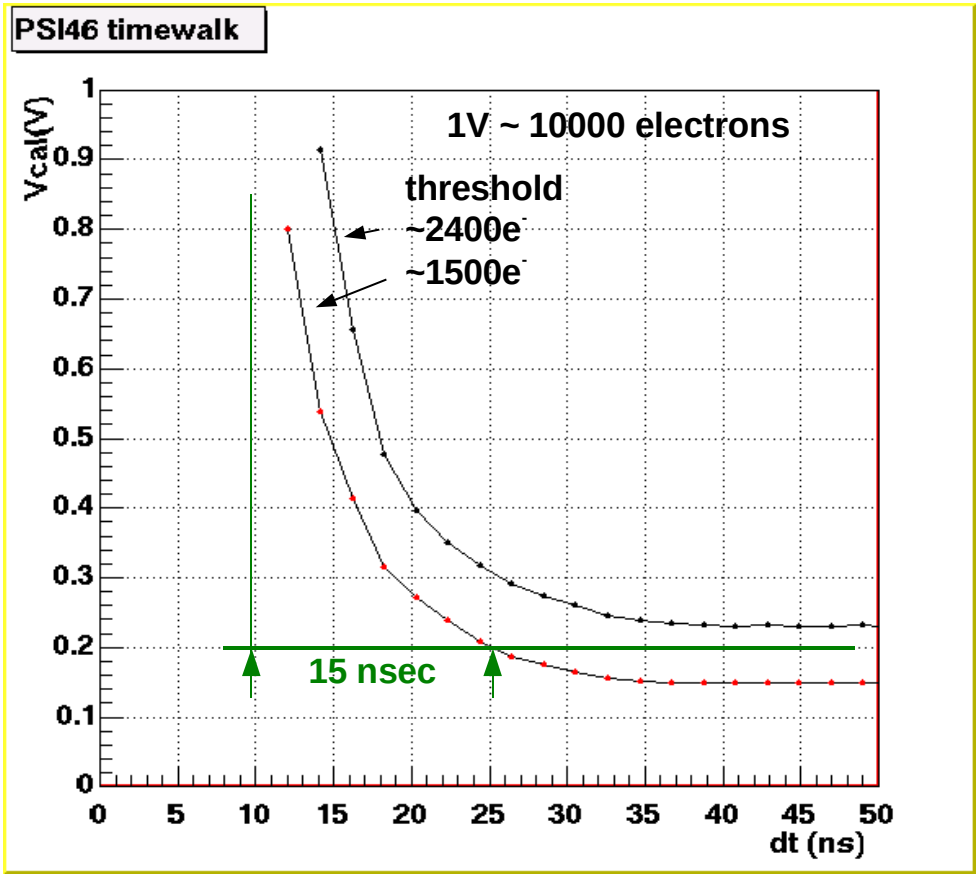
chipname	*DMILL_PSI43*	*IBM_PSI46*
CMOS technology	0.8 μm BiCMOS, SOI, 2 metals	IBM 0.25 μm, bulk, 5 metals
size of final ROC layout	7950 μm x 10800 μm	7900 μm x 9800 μm
pixel array	52 x 53 = 2756 pixels	52 x 80 = 4160 pixels
pixel size (rφ x z)	150 μm x 150 μm	100 μm x 150 μm
number of transistors	430 k	1280 k
number of supply pads	42 pads (150 μm pitch)	35 pads (175 μm pitch)
number of external capacitors	6	3
number of supply voltages	4 (5 V, 3.5 V, 3 V, 2.5 V)	2 (2.5 V, 1.75 V)
total supply current	160 mA	~ 70 mA

Timewalk of PSI46 (no sensor)



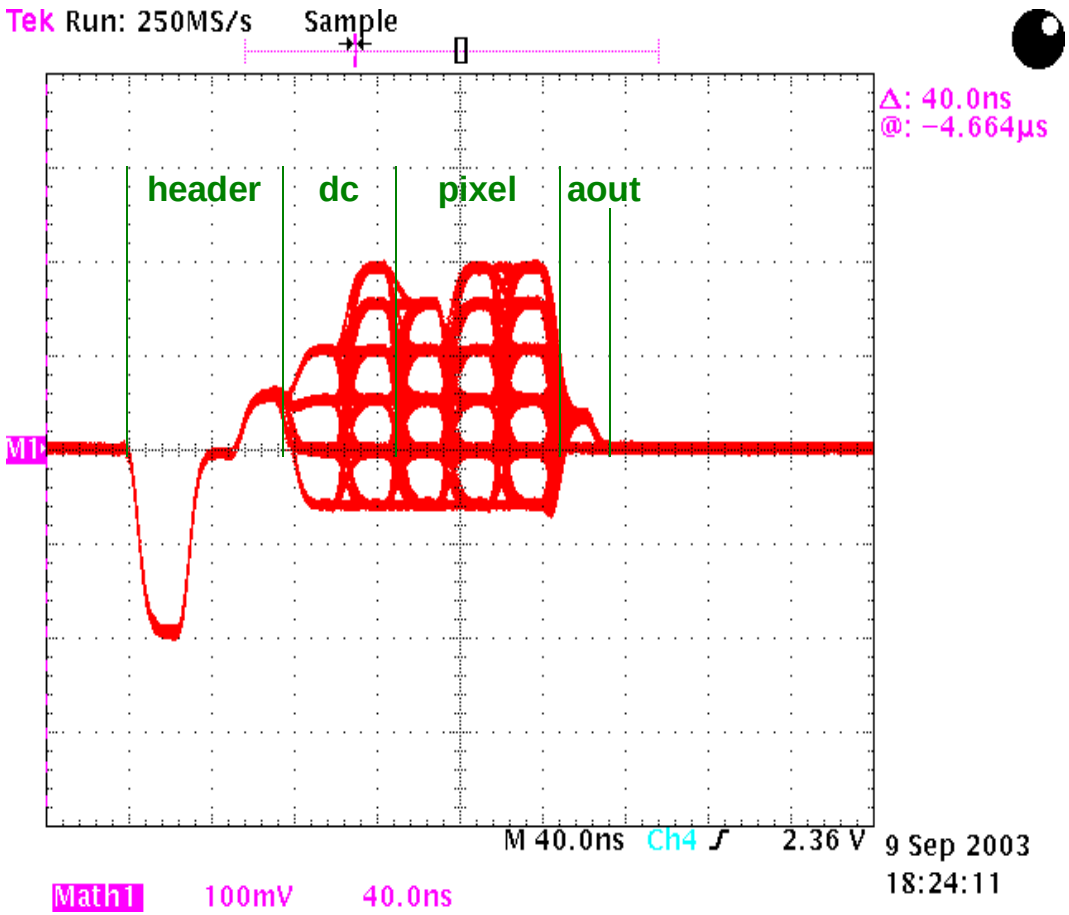
- **delay due to raise time of analog signal**

⇨ **timewalk < 20ns**



analog readout of PSI46

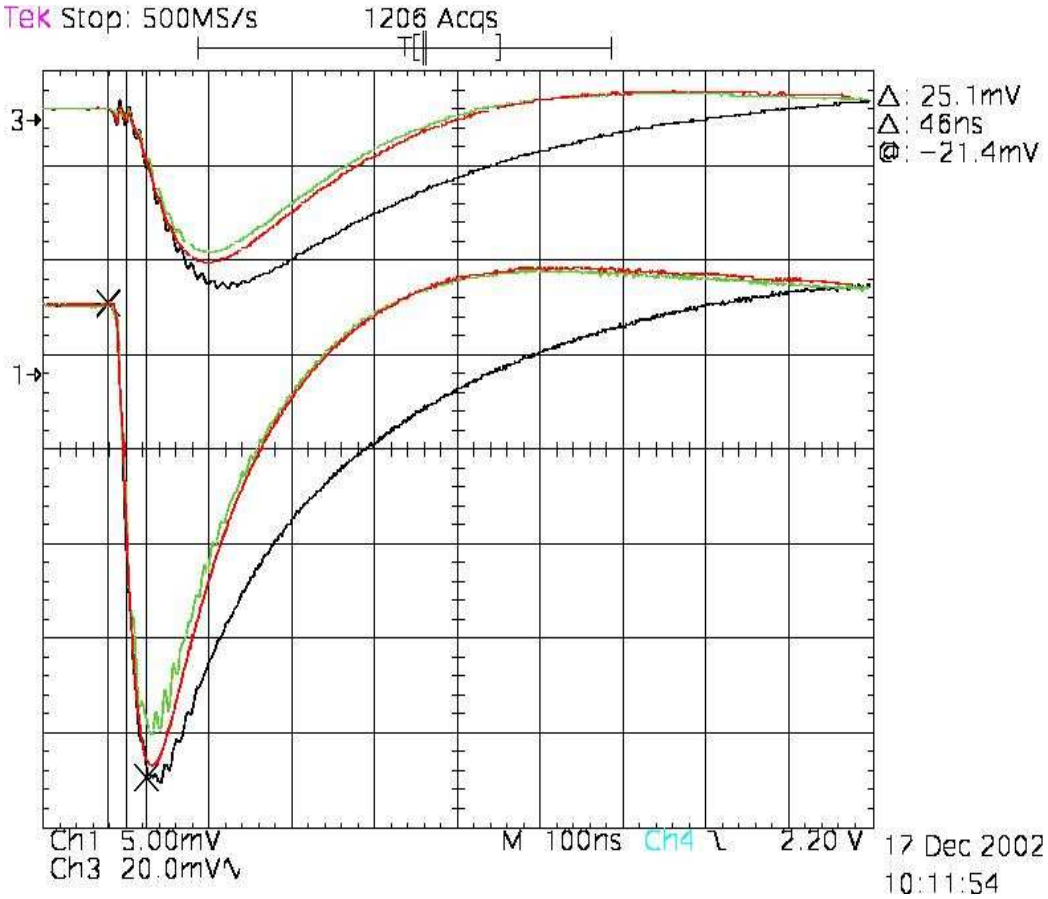
- **40 MHz, 20 MHz fallback**
- **3 cycles header per chip**
- **addresses analog coded**
  - **6 levels**
  - **2 cycles double column**
  - **3 cycles pixel row**
- **1 cycle analog pulse height**
- **repeated for each hit**
- **each readout pass returns data for only one trigger number**



Radiation Tolerance of DSM teststructure

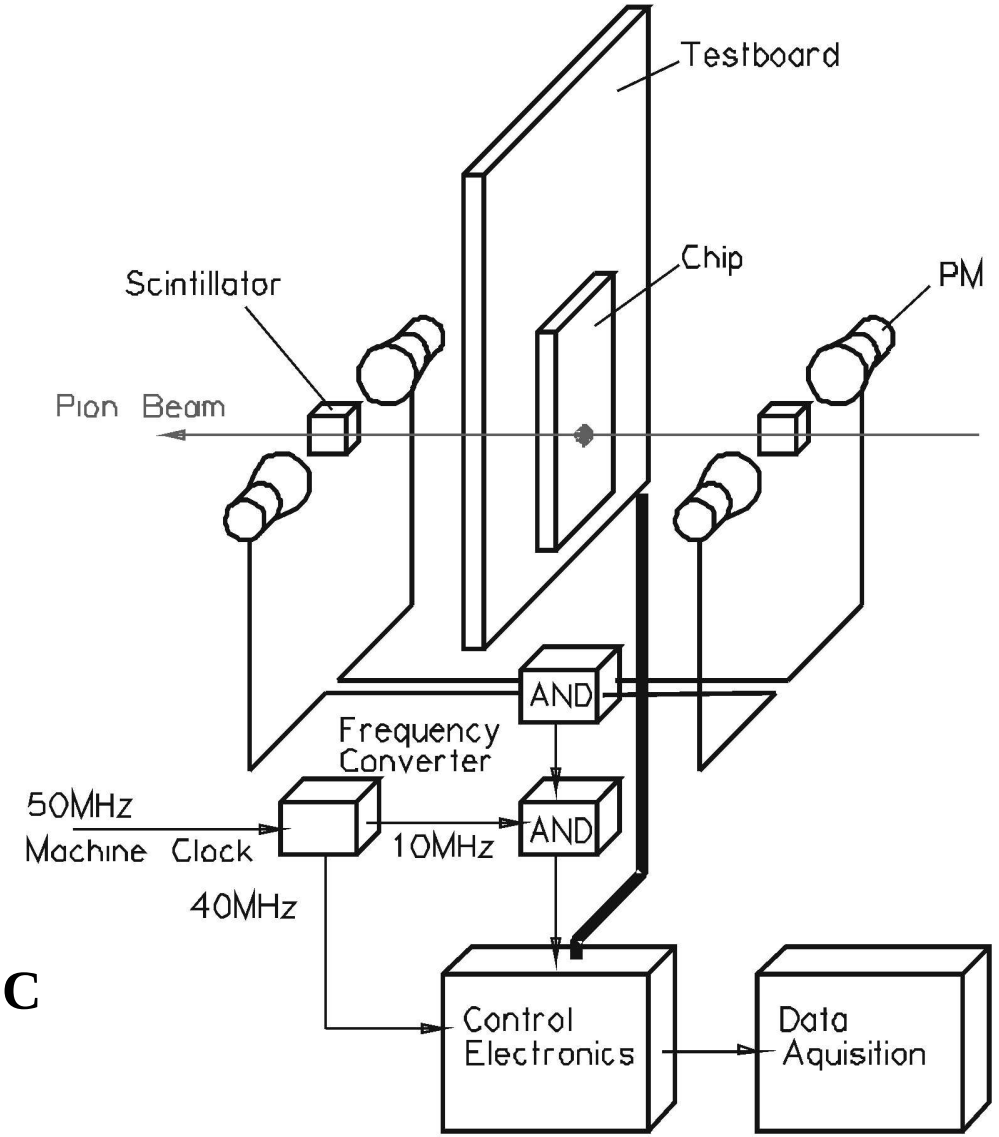
- **teststructure of the analog block**
- **effects of radiation**
  - **before irradiation**
  - **after irradiation (13.2 Mrad)**

⇨ **compensate irradiation effects by readjusting feedback**



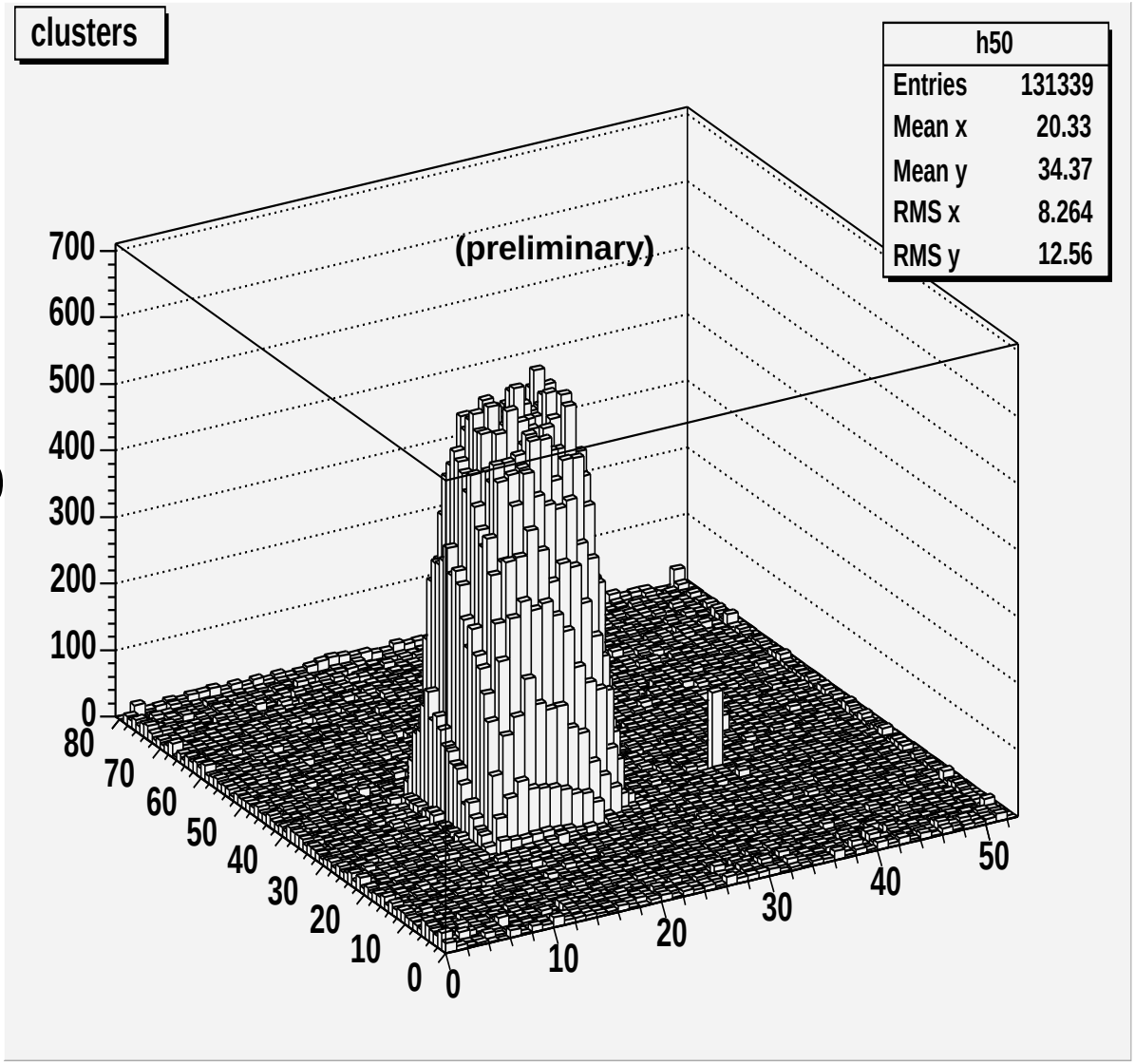
PSI Testbeam Setup September 2003

- **beamline πE1 at PSI:**
  - **π^--beam, 300 MeV/c**
  - **50 MHz bunch structure**
- **beam intensity variable up to 80 MHz/cm^2**
- **trigger:**
  - **scintillators**
  - **size 2*2*2 mm^3 cubes**
- **goal of testbeam:**
  - **data loss under LHC equivalent conditions**
  - **general functionality of DSM ROC**



PSI46 performance

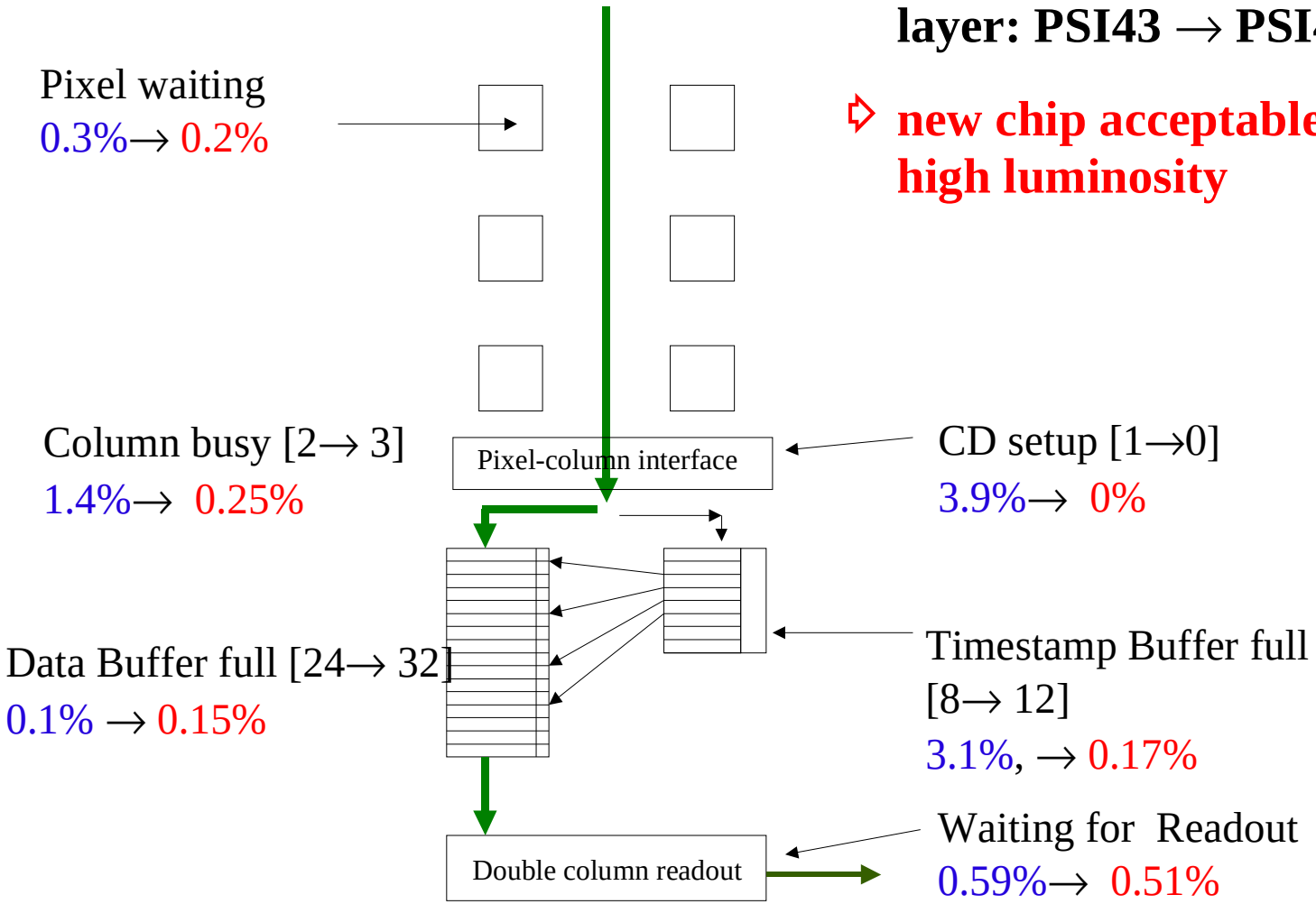
- **single PSI46 ROC bump-bonded to a 280 μm thick silicon sensor**
- **hit map for events triggered with scintillators (2mm*2mm)**
- **chip clock 40 MHz**
- **digital address encoding works fine**



data loss mechanisms of PSI43 and PSI46

- **Data loss simulations for LHC conditions, full luminosity for 4cm layer: PSI43 → PSI46**

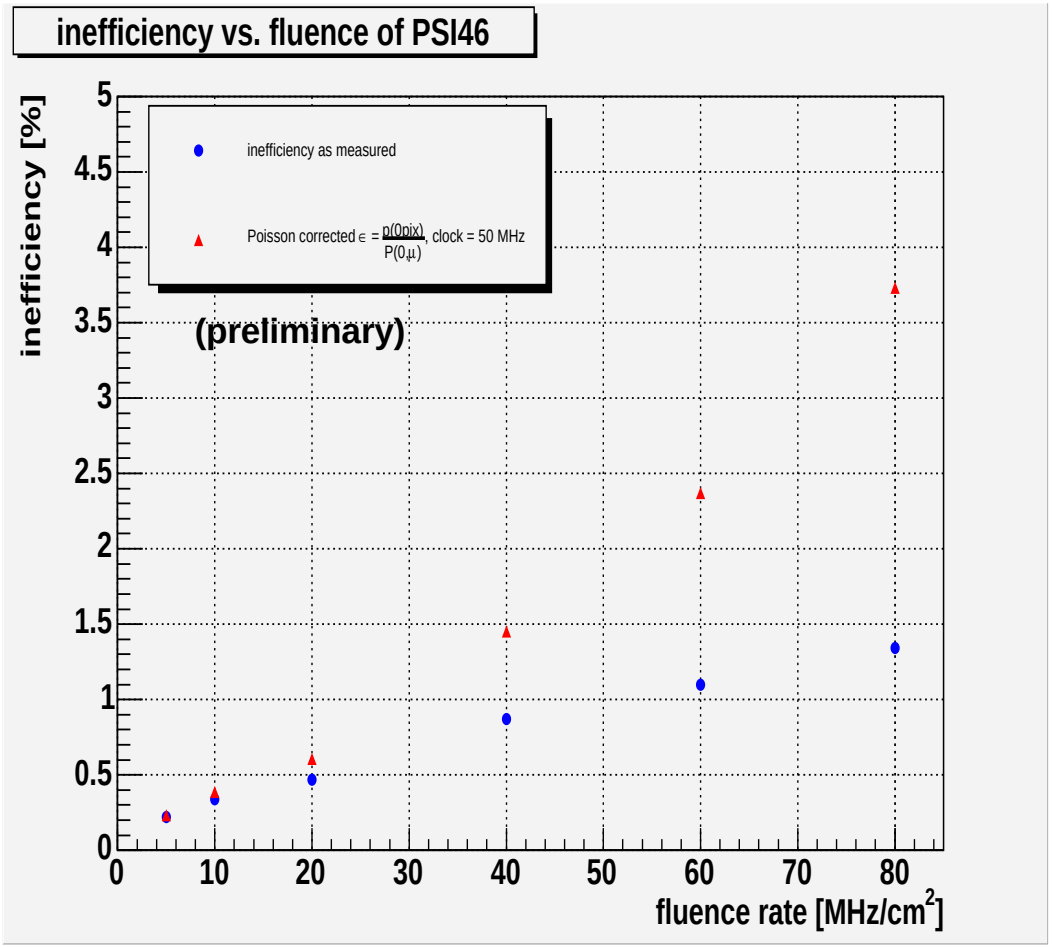
⇨ **new chip acceptable for inner layer @ high luminosity**



inefficiency for beam particles of PSI46

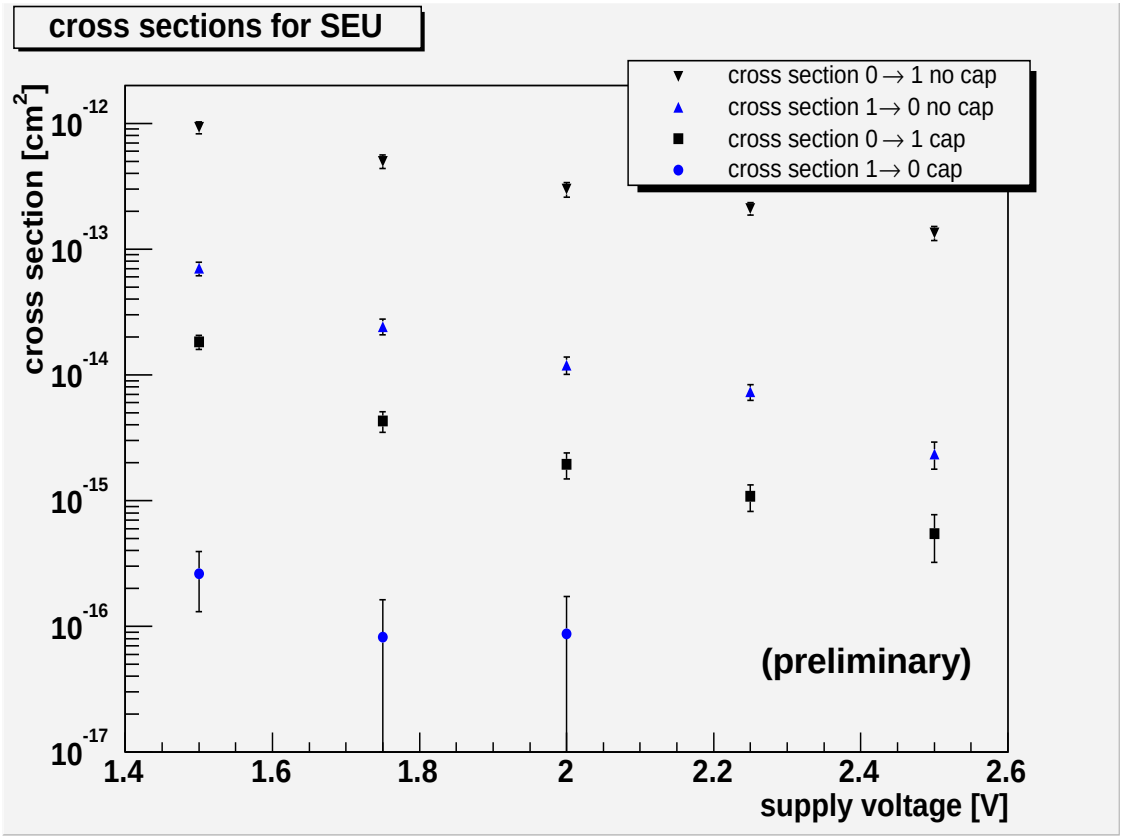
- **comparator threshold 2500e$^-$**
- **inefficiency like expected according to simulations e.g. 1.3%@ 40MHz**

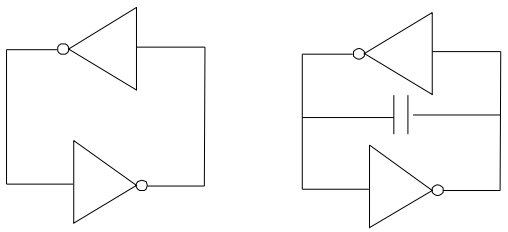
⇨ **no additional data loss seen**



Single Event Upset (SEU) for SEU teststructure

- **flipping of bits due to deposited charge**
- **requires permanent reloading of trimbits**
- **standard FF: $\sigma=3*10^{-13}\,cm^2$**
  - **need to reload 16pixels/s per control link**
- **protected FF: $\sigma=2*10^{-15}\,cm^2$**
  - **need to reload 0.1 pixels/s per control link**
  - **manageable**





Conclusions/ Outlook

- **successful translation of the DMILL readout chip to 0.25 μm**
- **significantly improved over PSI43**
- **first chips tested, looks very good**
- **some minor problems identified, know how to fix**
- **re-submission with minimal changes early 2004**